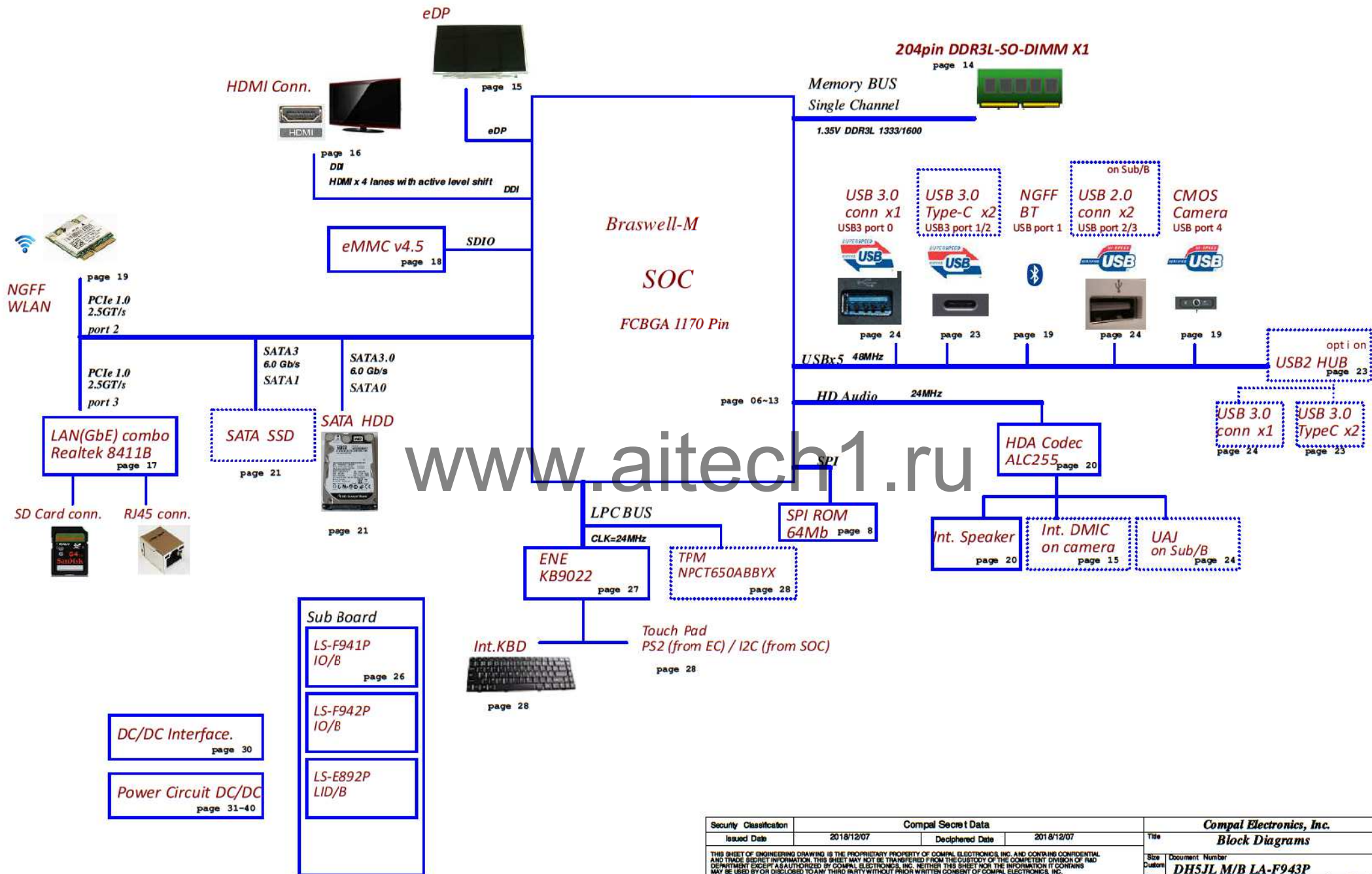


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**DH5JL MB Schematic Document**  
**LA-F943P**

**Rev: 1.0**

**2017.12.07**

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Size	Document Number	Rev	1.0	
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Power Plane	Description	S0	S3	S4/S5
+19V_VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTC_VCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	OFF
+1.15VALW	+1.15v Always power rail	ON	ON	OFF
+1.24VALW	+1.24v Always power rail	ON	ON	OFF
+1.8VALW	+1.8v Always power rail	ON	ON	OFF
+3VALW	+3.3v Always power rail	ON	ON	OFF
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35v power rail for DDR3L	ON	ON	OFF
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VGG	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
SOC_I2C5 +3VALW	Touch Pad SA577C-1202 (ELAN)	0x15		
	Touch Pad TM-P3218-001 (SYNAPTICS)	0x2C		
PCU_SMB +3VLAW	DIMM1	0xA0		
EC_SMB_CK1 +3VLP_EC	ISL88739AHR(Charger IC)	0x09		
	BATTERY PACK	0x16		
EC_SMB_CK2 +3VS	Thermal_sensor	0x9E		
	TYPEC			

941@  
ZZZ PCB DHUL LA-F941P

Part Number	Description
DA6001WY000	PCB DHUL LA-F941P

Part Number	Description
DA6001Y0000	PCB DHJL LA-P942P

Part Number	Description
DA6001Y3000	PCB DHJL LA-P943P

Part Number	Description
DAZ2A00100	PCB DH5JL LA-F943P LS-F941P/E992P

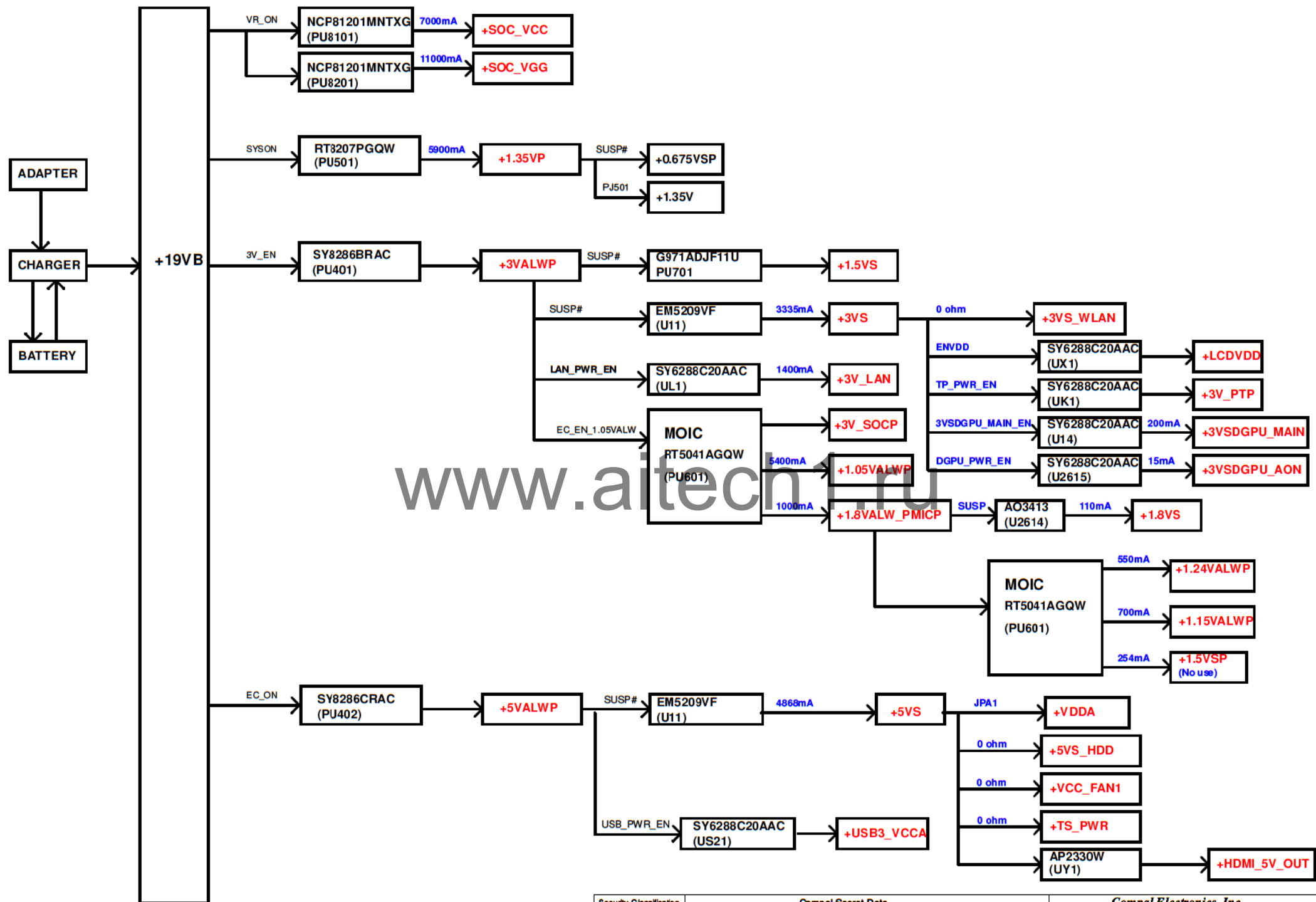
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.534V	1.550V	1.567V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE
19	NC	3.000V	3.300V		0xF7 - 0xFF

Board ID	PCB Revision
00	EVT_LA-F943PR01
01	PVT_LA-F943PR10
02	PreMP_LA-F943PR10
04	

43 Level	Description	BOM Structure
431A8LBOL02	SMT MB AF943 DH5JL N3060 SR2KN HDMI	NCHG@/NHUB@/SR2KN@/TMS@/PVT@/DAZ@/
431A8LBOL03	SMT MB AF943 DH5JL N3060 OFF SR2ZN HDMI	NCHG@/NHUB@/SR2ZN@TMS@/PVT@/DAZ@/
431A8LBOL04	SMT MB AF943 DH5JL N3160 SR2KP HDMI	NCHG@/NHUB@/SR2KP@TMS@/PVT@/DAZ@/
431A8LBOL05	SMT MB AF943 DH5JL N3710 SR2KL HDMI	NCHG@/NHUB@/SR2KL@TMS@/PVT@/DAZ@/

BOM Option Table		BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure	Item	BOM Structure
Unpop	@	CPU N3060	SR2KN@		
Connector	CONN@	CPU N3160	SR2KP@		
EMC requirement	EMC@	CPU N3710	SR2KL@		
EMC requirement depop	@EMC@	USB3-TYPEC	TYPEC@		
Power Button	DBG@	EMC TYPEC	EMC_TYPEC@		
TPM	TPM@	USB2-Charger	CHG@		
USB HUB	HUB@				
eMMC parts	EMMC@				
LAN SWR mode	SWR@				

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				Date	Wednesday, December 06 2017
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## DH5JL\_EVT Power Sequence AC mode

BIOS ver: V0.01

EC: ver: V0.01

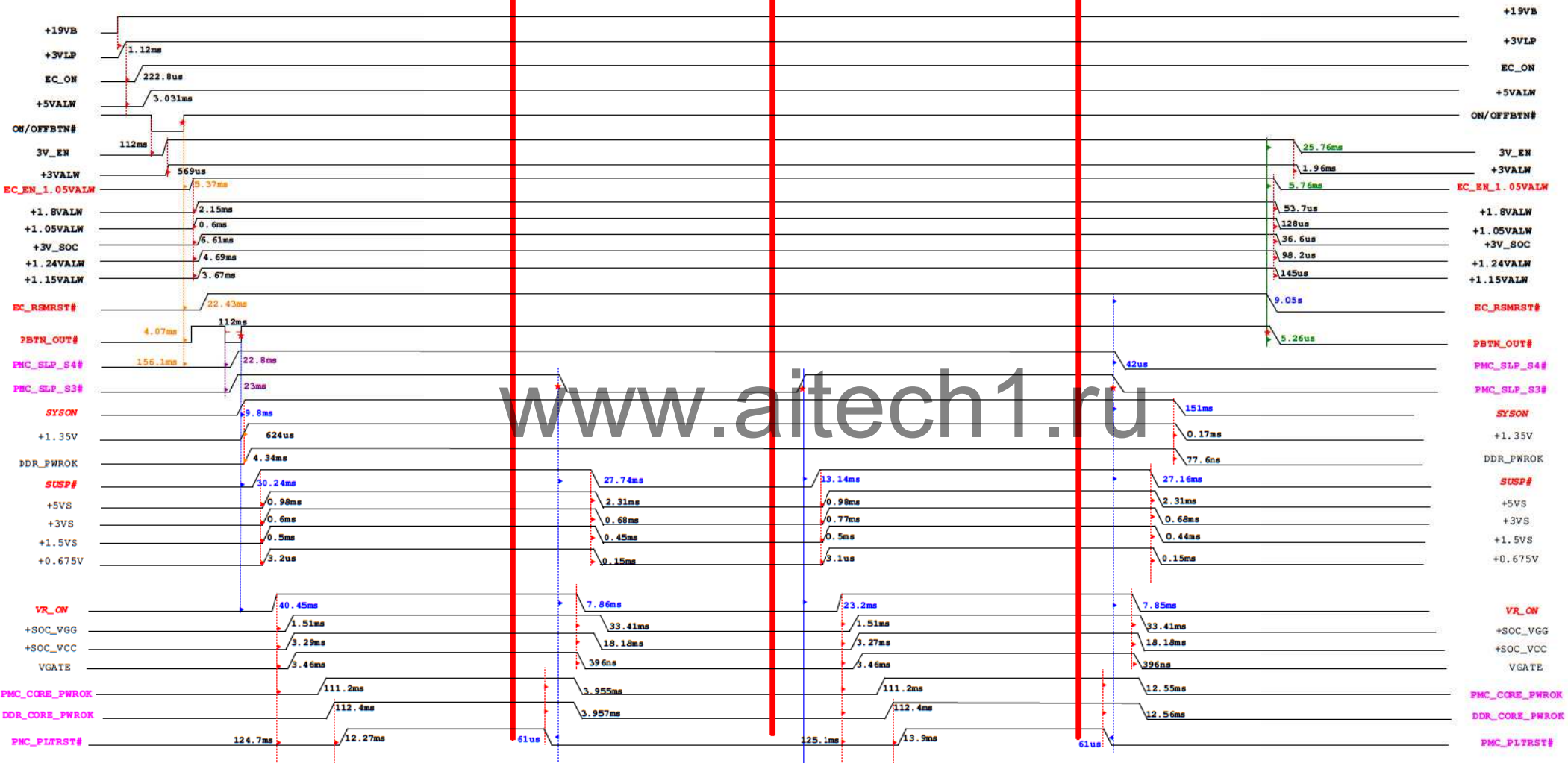
Plug in

Power On

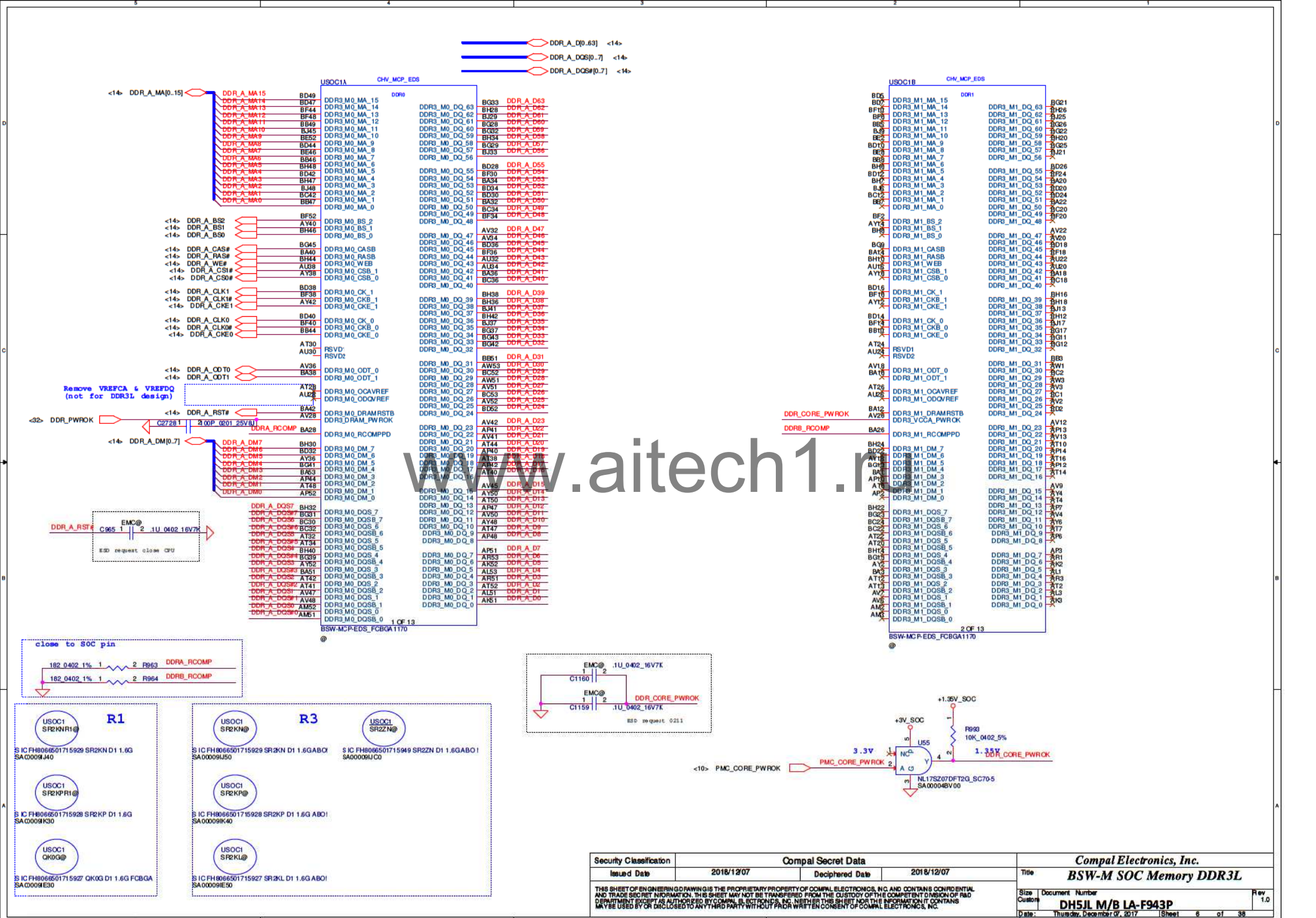
S3

S3 Resume

Power Off



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DH5JL M/B LA-F943P				Rev 1.0
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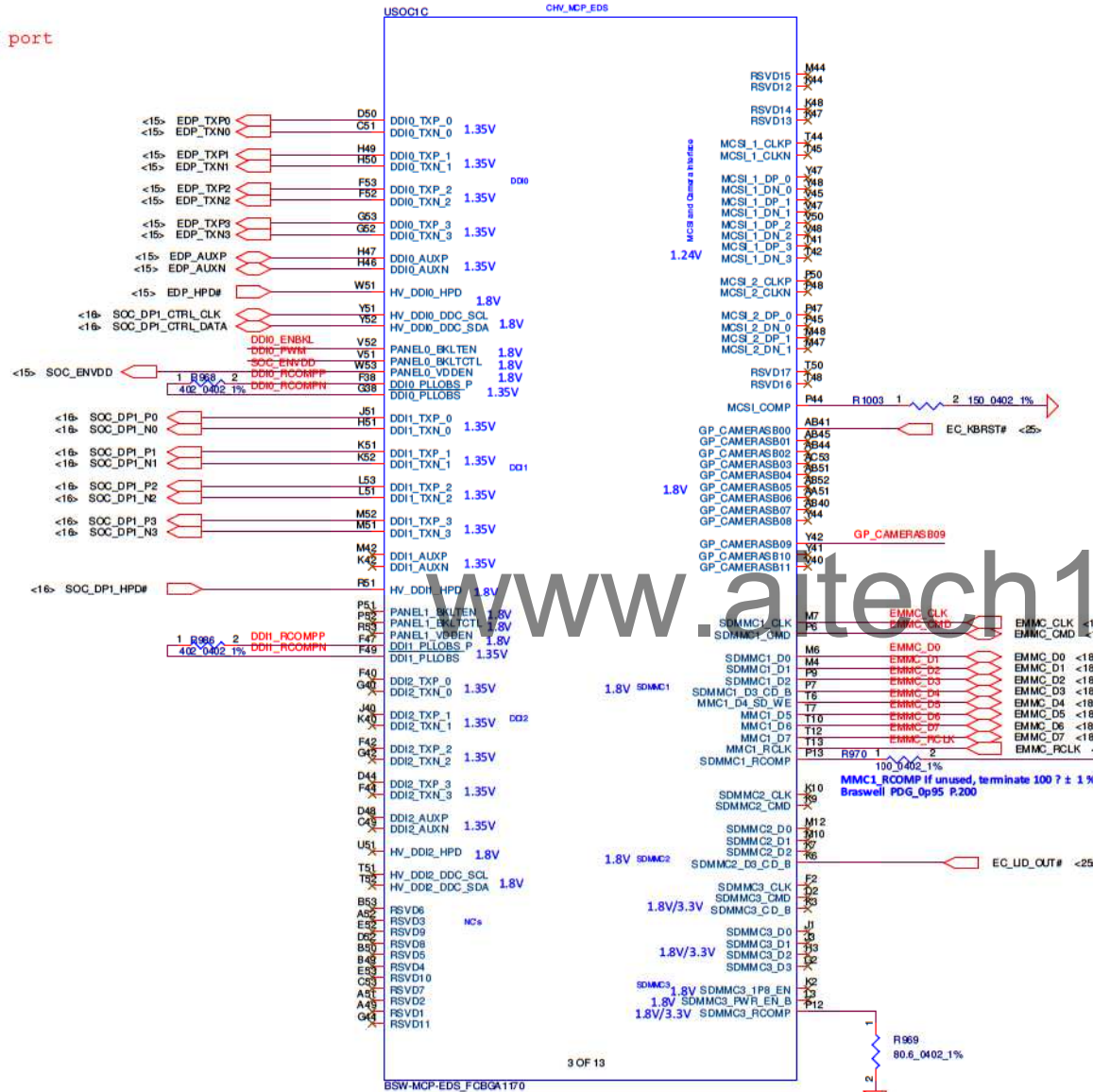


EDP /HDMI change port

EDP

HDMI

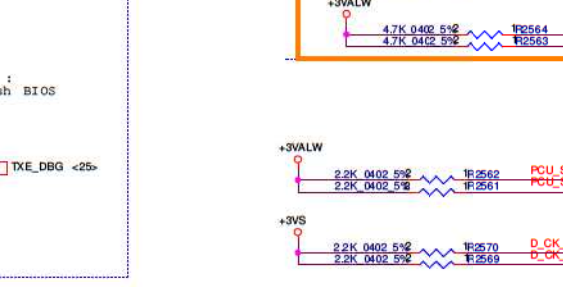
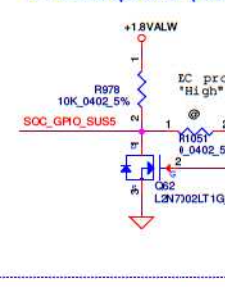
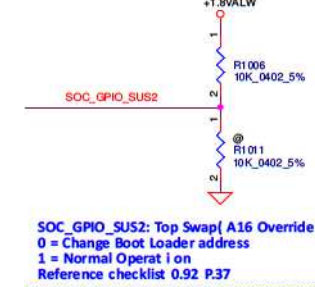
HPD low active



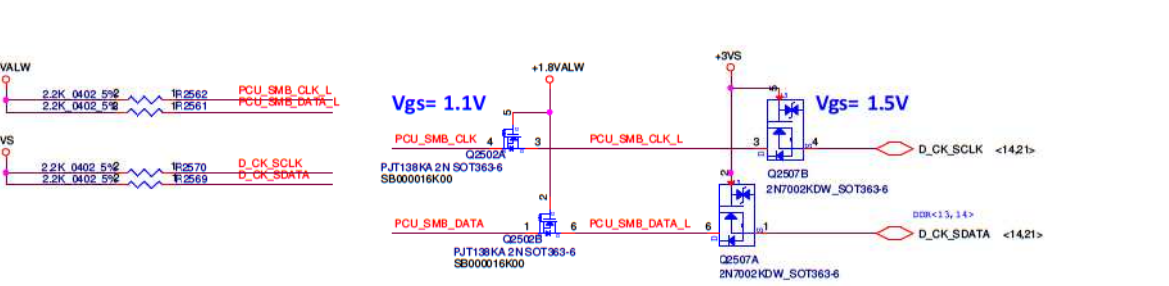






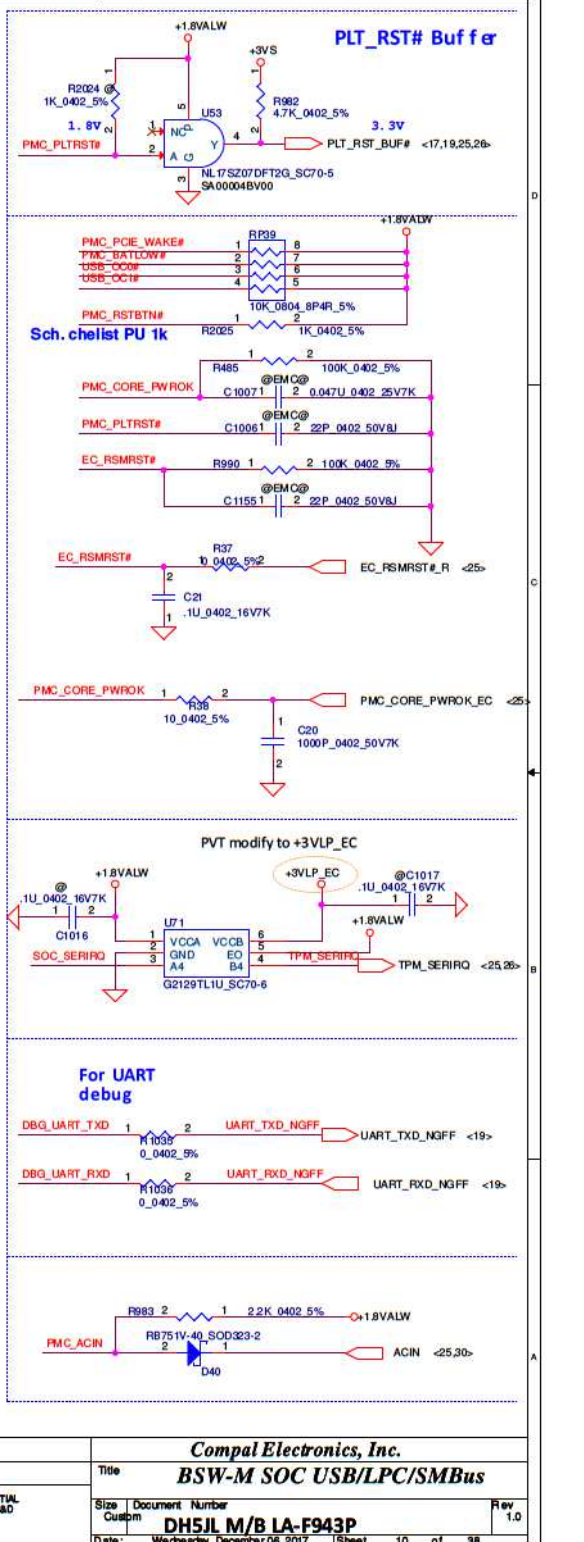
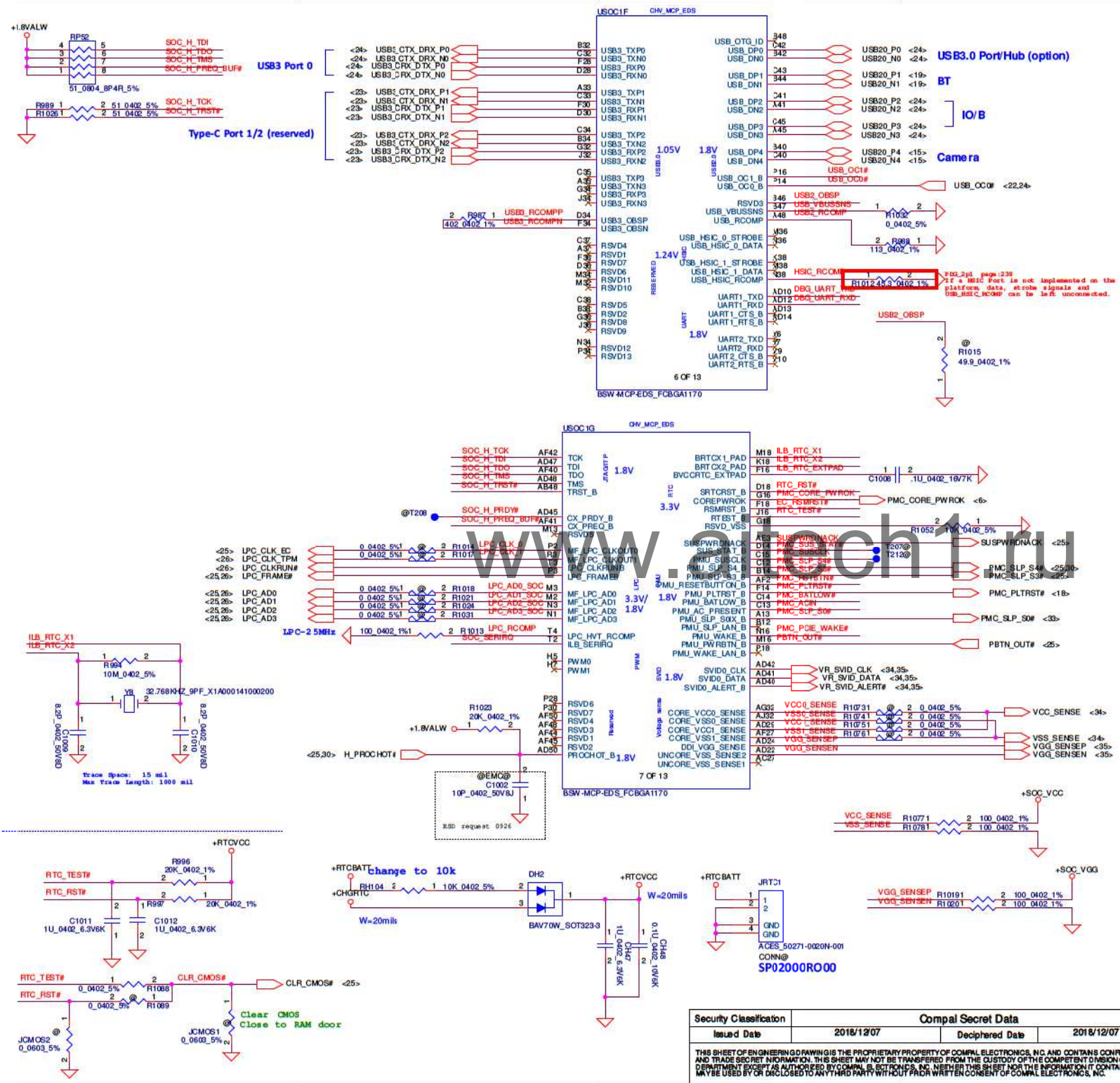


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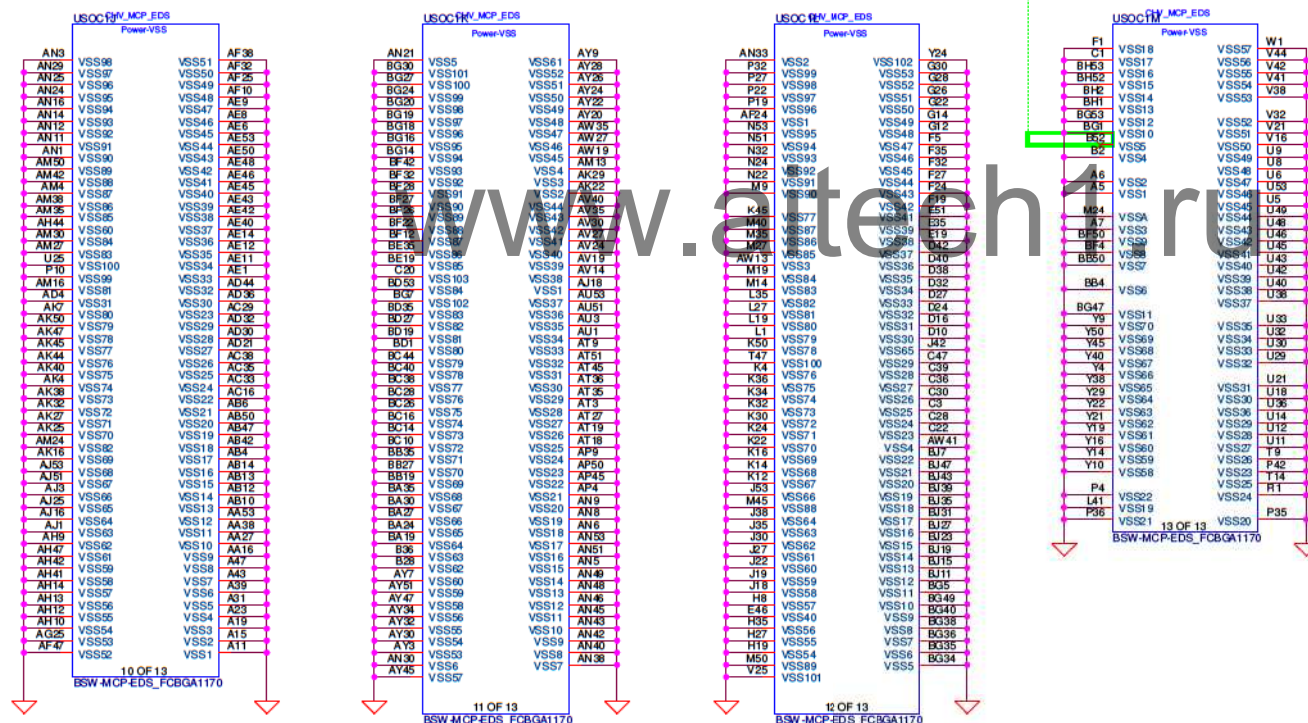
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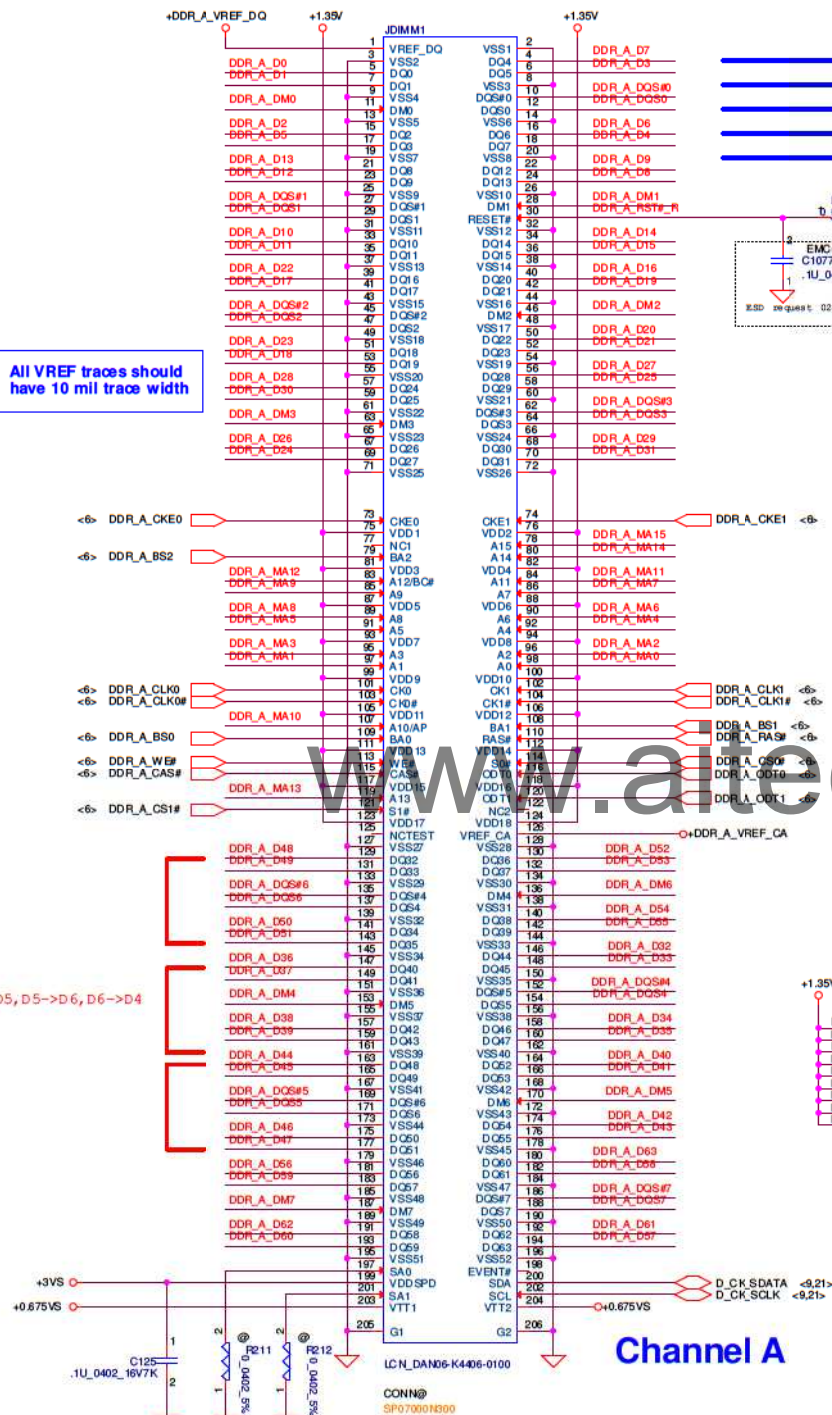




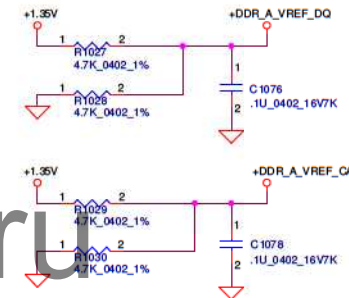
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All VREF traces should have 10 mil trace width

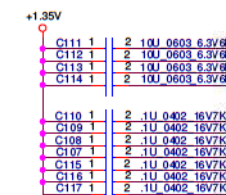
Swap D4->D5, D5->D6, D6->D4



Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO DIMMS ON DIMM\_VREF\_CA / DIMM\_VREF\_DQ  
Decoupling caps are needed; one 0.1  $\mu$ F placed close to VREF pins of each DDR3 SODIMM.



Layout Note:  
Place near JDIMM1



Layout Note:  
Place near JDIMM1.203,204



<Address: SA1:SA0=00 (A0H)>

DIMM\_1 Standard

Channel A

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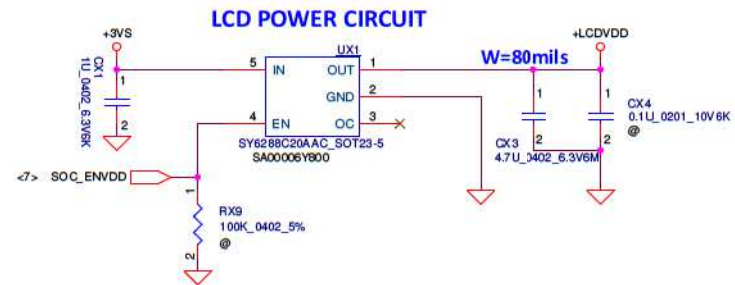
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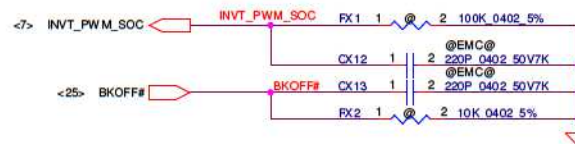
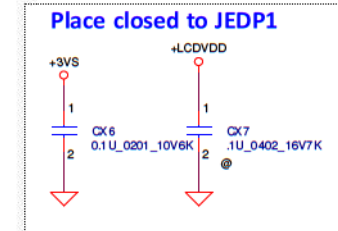
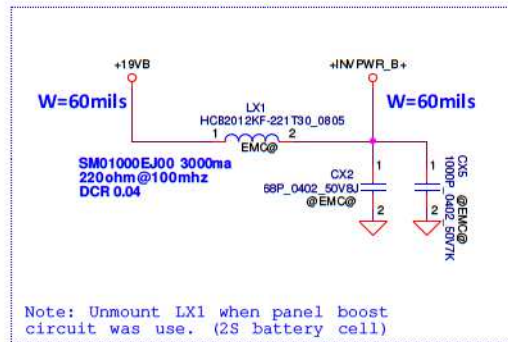
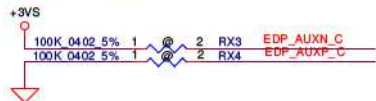
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Size: Document Number: DH5JL M/B LA-F943P

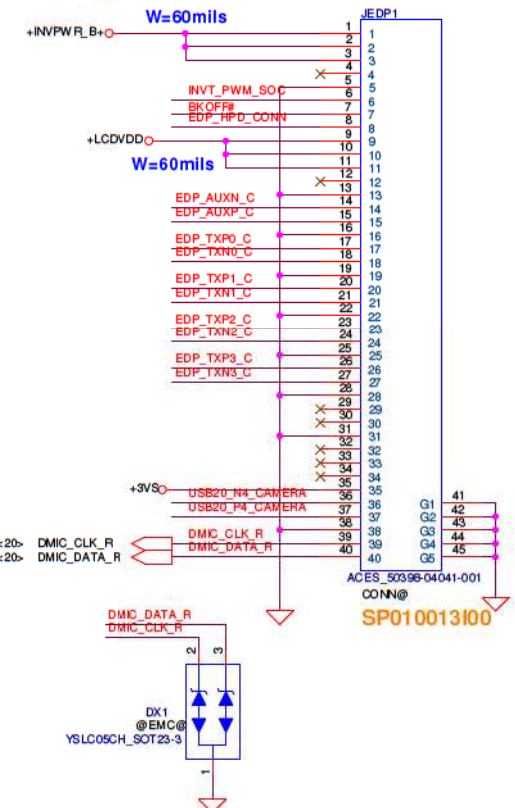
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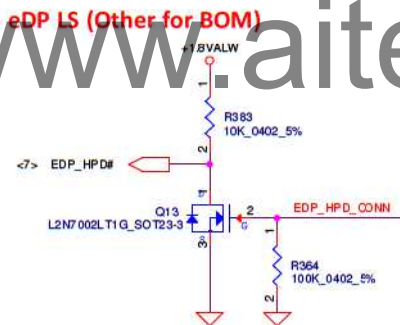
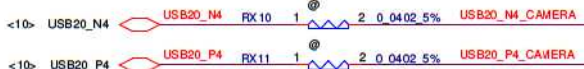
if support 4k panel, CX16-CX19 need be soldered



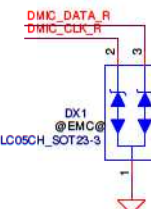
## LED PANEL Conn.



## Camera



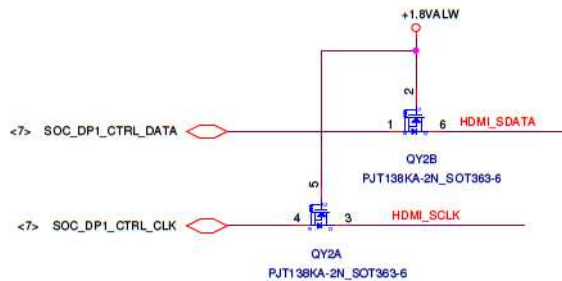
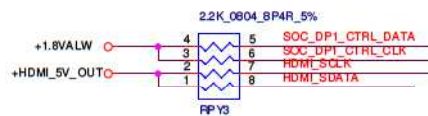
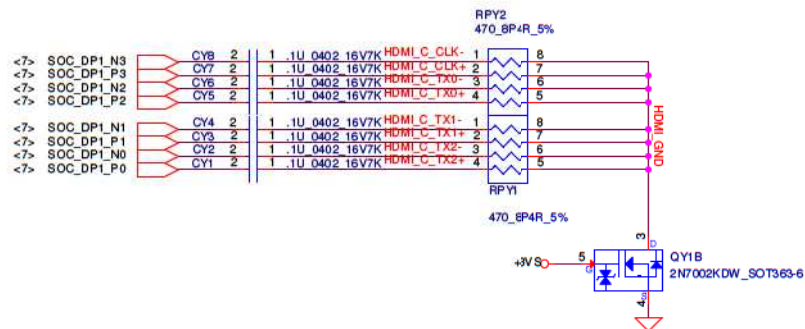
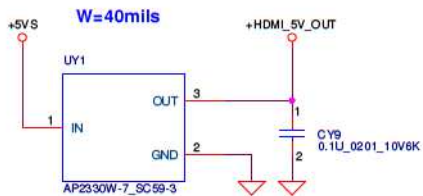
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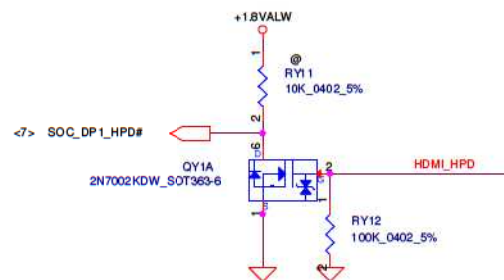
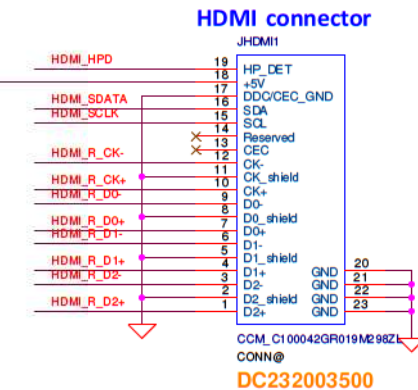
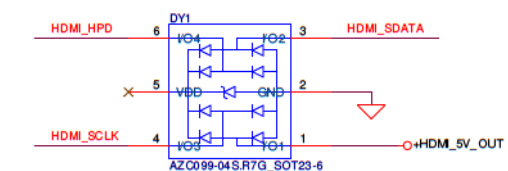
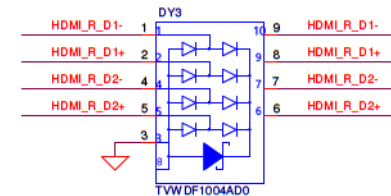
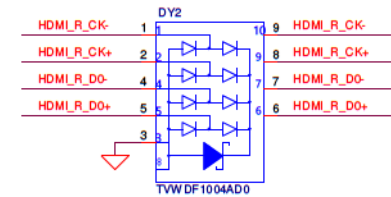
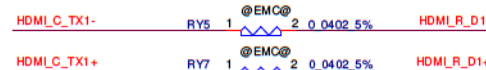
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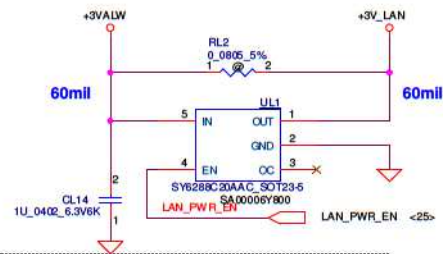
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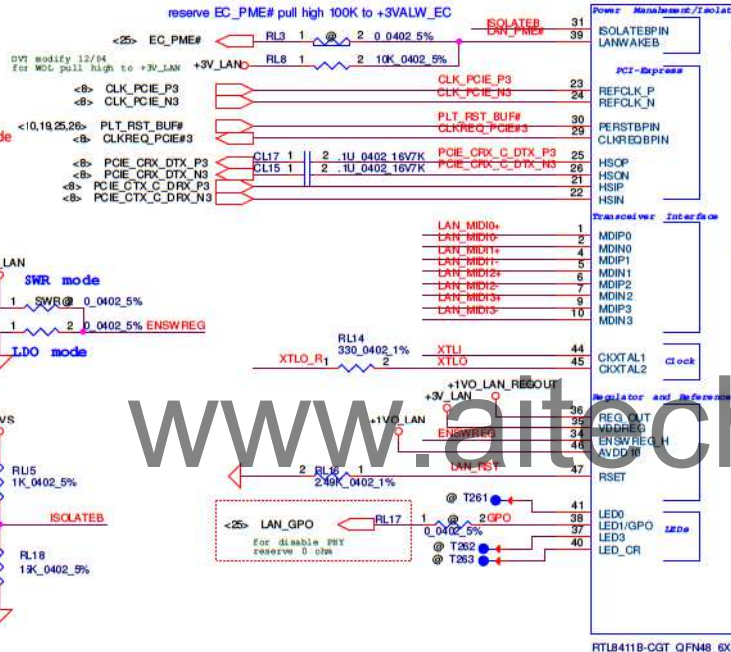
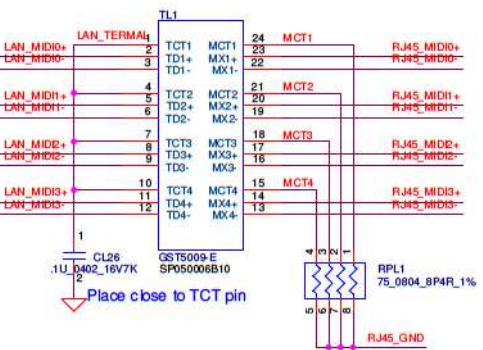
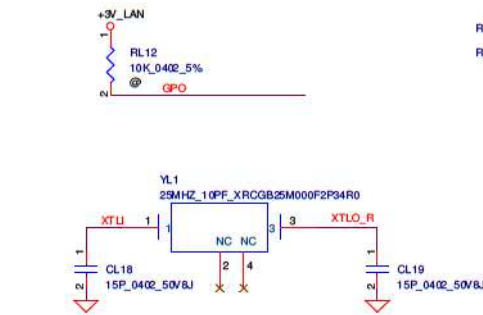
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# LAN-RTL8411B

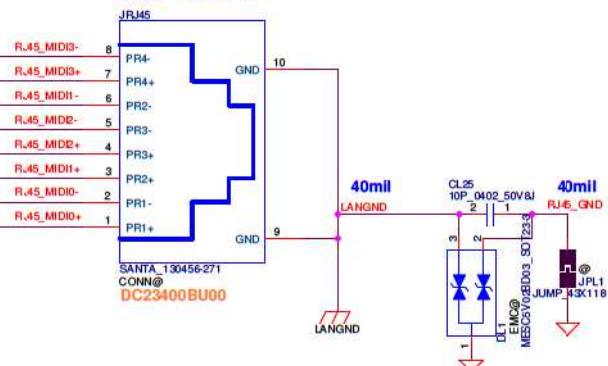


From EC  
High active.  
EN threshold voltage min:1.2V  
typ:1.6V max:2.0V  
Current limit threshold 1.5-2.8A  
+3V\_LAN Rising time must >0.5ms and <100ms

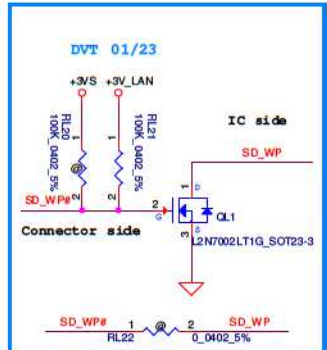


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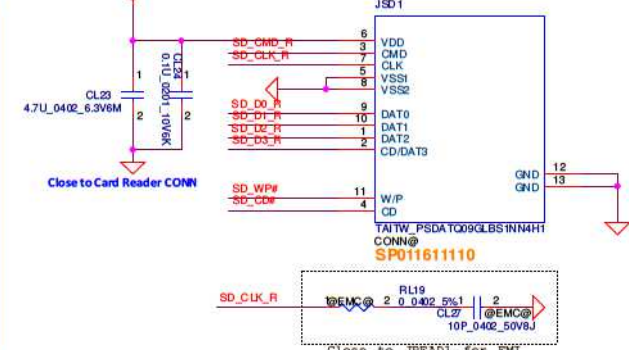
## LAN Connector



## SD Write protect inverter circuit



## Card Reader Connector



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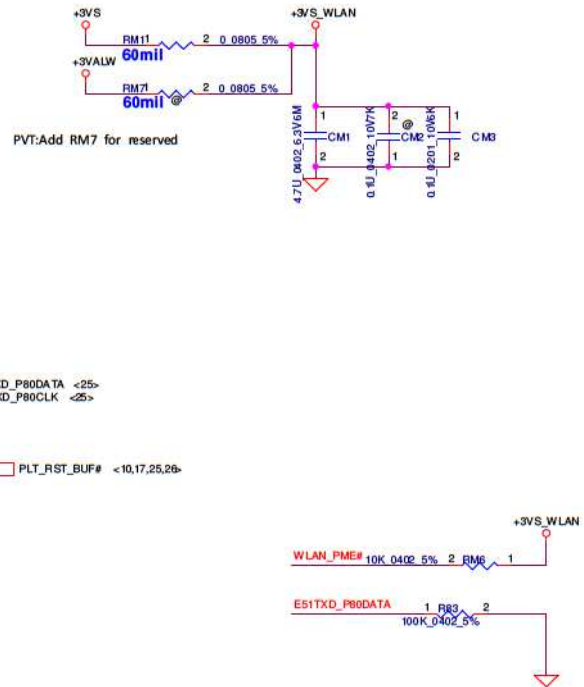
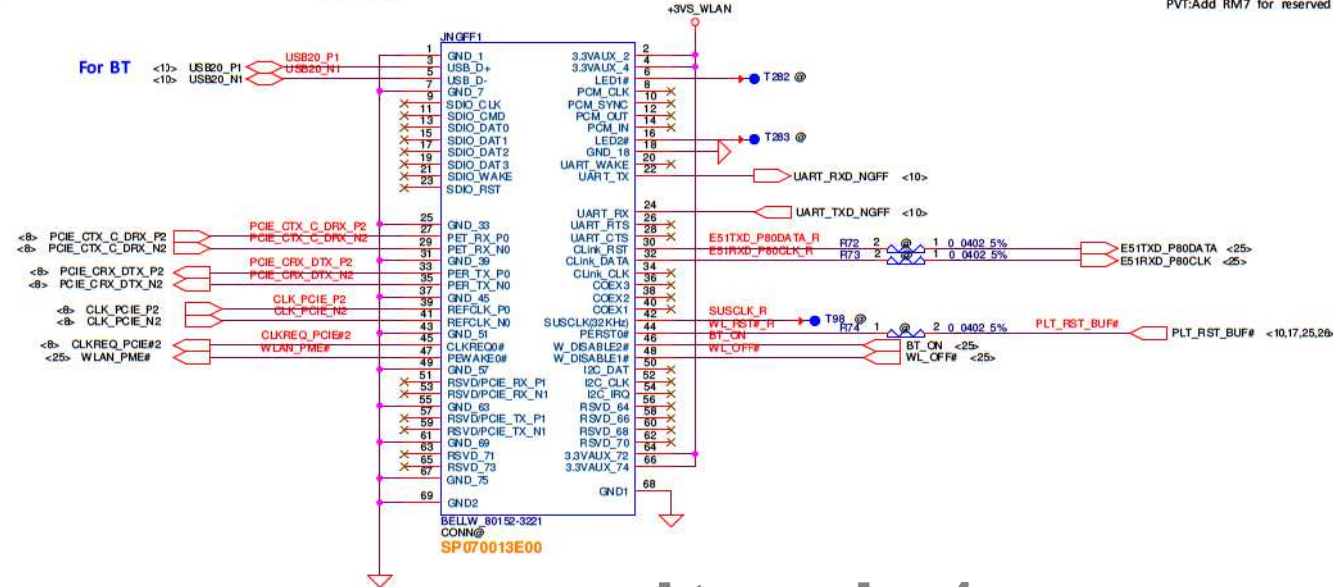




# Wireless LAN

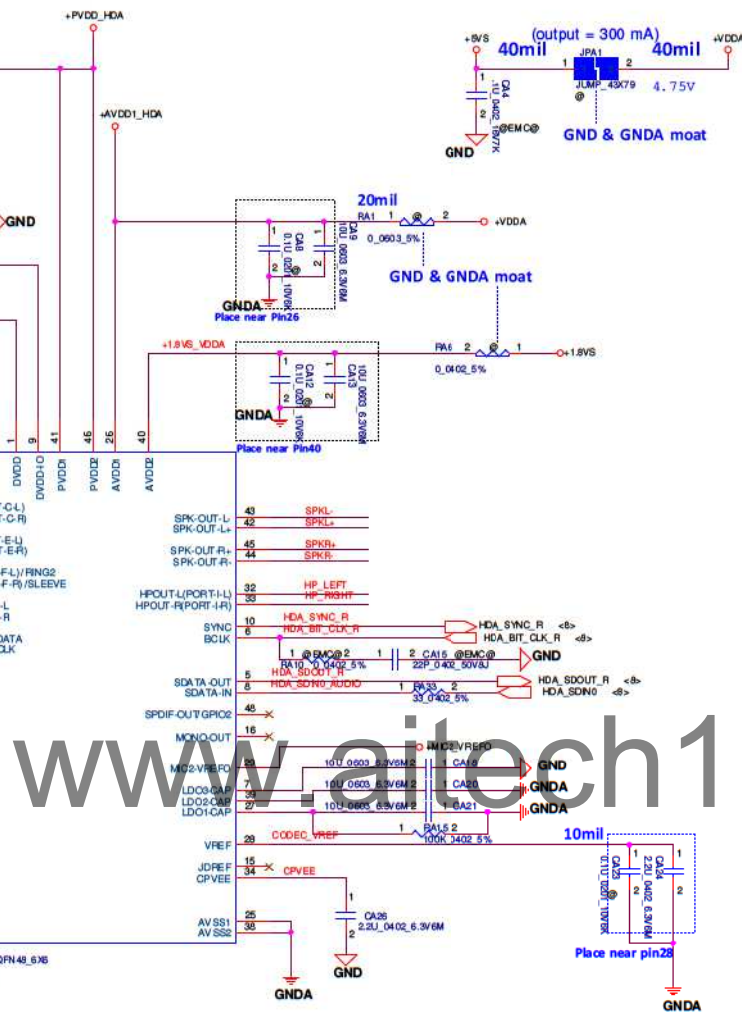
NGFF WL+BT (KEY E)

KEY E



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Issued Date				2018/12/07				Title			
Deciphered Date				2018/12/07				M.2 Key E (WLAN)			
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				DH5JL M/B LA-F943P				1.0			
Date: Wednesday, December 06 2017				Sheet 19 of 38							

[illegible][illegible]

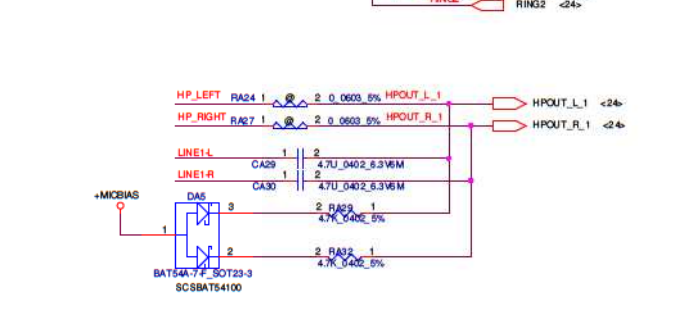
TO eDP Conn

DMIC\_DATA 2 1 RA35 DMIC\_DATA\_R DMIC\_DATA\_R <15>

DMIC\_CLK 2 1 0.0402, 5% DMIC\_CLK\_R DMIC\_CLK\_R <15>

DMC15PXP221 SN1D

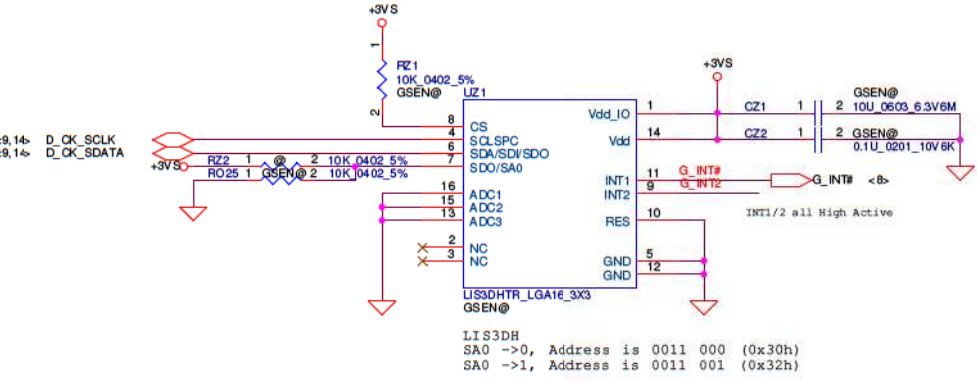
$+MC2\_VREF0$   
 $RA19$   
 $2.2K\_0.400\_5\%$   
 $RA20$   
 $2.2K\_0.400\_5\%$   
 $SLEEVE$   
 $SLEEVE <24p$



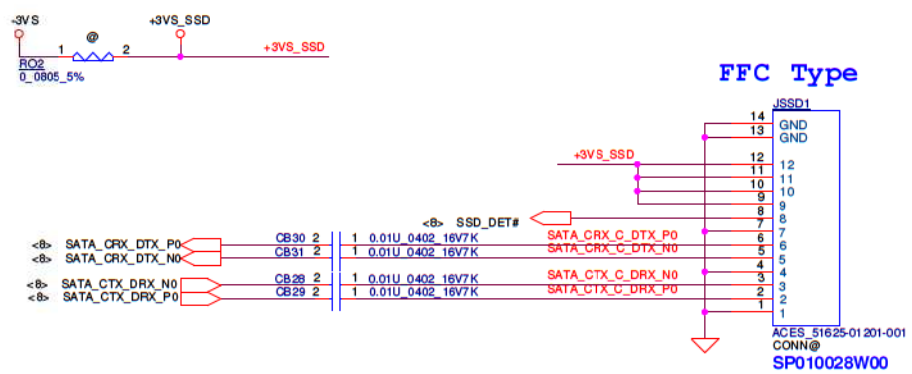
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Issued Date		2018/12/07	Deciphered Date		2018/12/07	
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				HD Audio Codec ALC255		
				Size	Document Number	
				Quater	DH5JL M/B LA-F943P	
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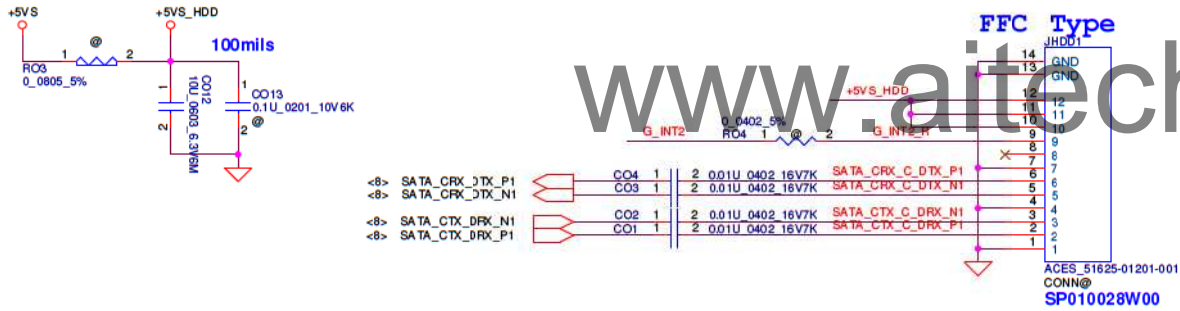
G-Sensor (Reserved)



SATA SSD Conn.



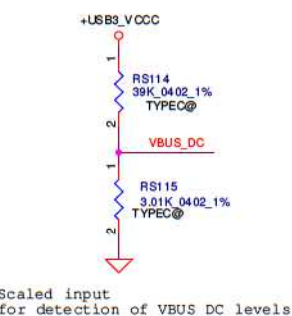
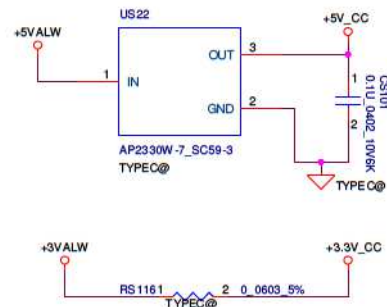
SATA FFC HDD Conn.



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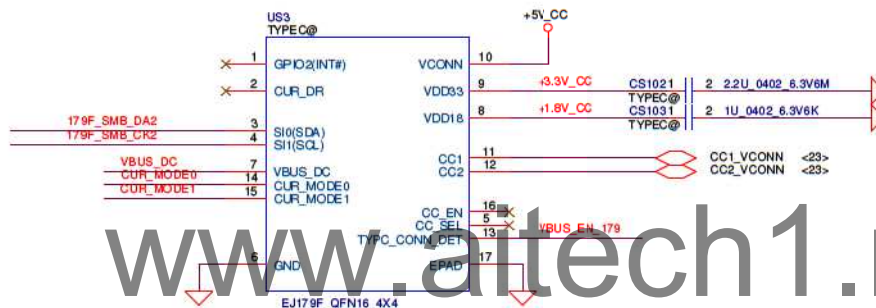
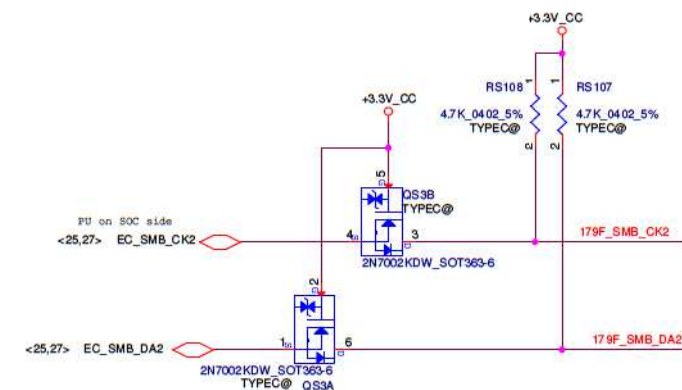
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/12/07		Deciphered Date	
2018/12/07		2018/12/07		Title	
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				1.0	

## TYPE C (Reserved)

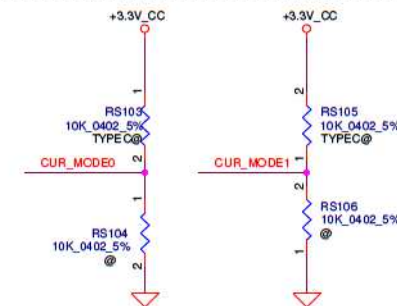


Remove INT#,  
platform doesn't monitor it  
report CC1 or CC2 is connection  
CC\_EN  
power path control "low active"

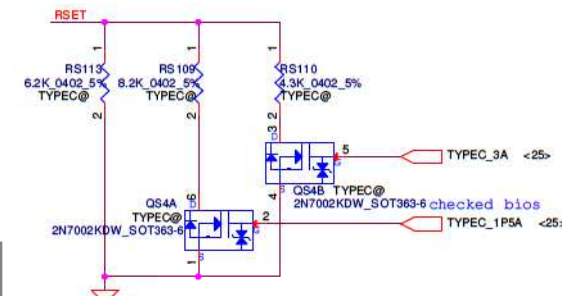
EC need change to low active



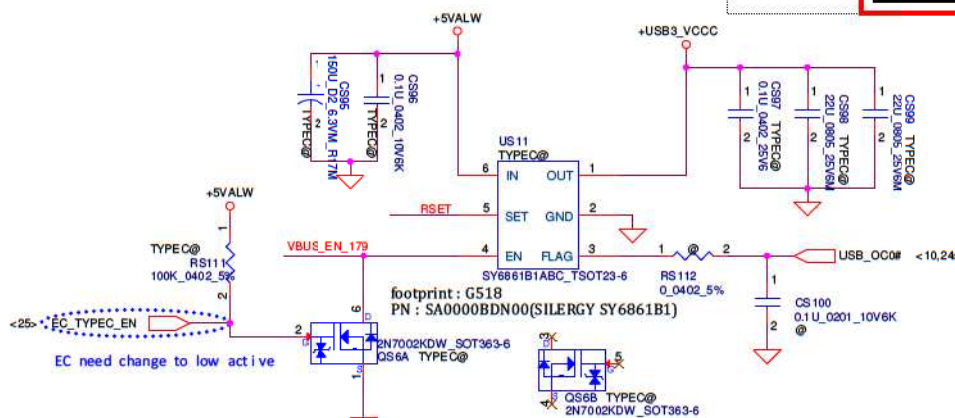
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Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



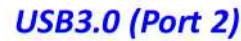
G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
H	H	1.94	3A	3.5A



Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

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### USB3.0 (Port 1)



For ESD request



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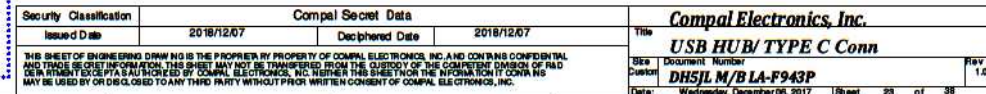
Port 1/2 is removable.

25.32 SYSON

USB3/IO (Type C)

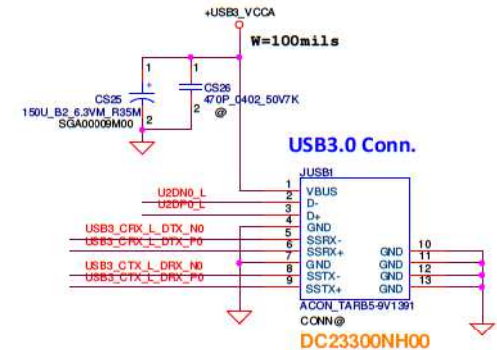
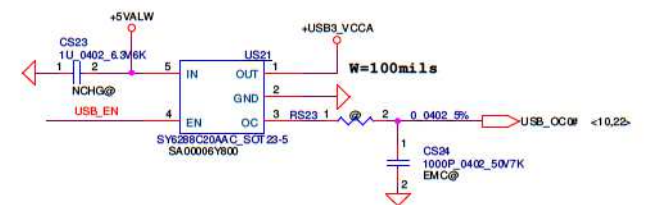
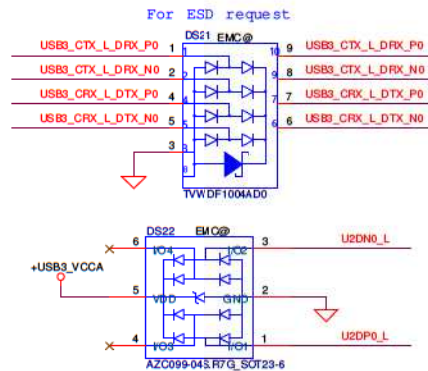
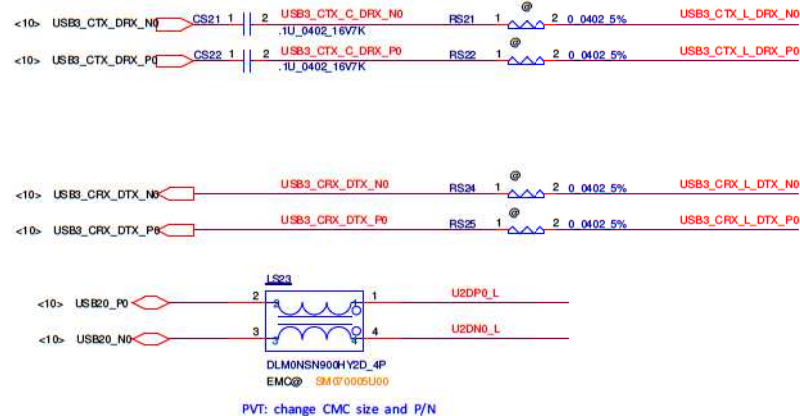
Port4 disable.

Port2 is removable



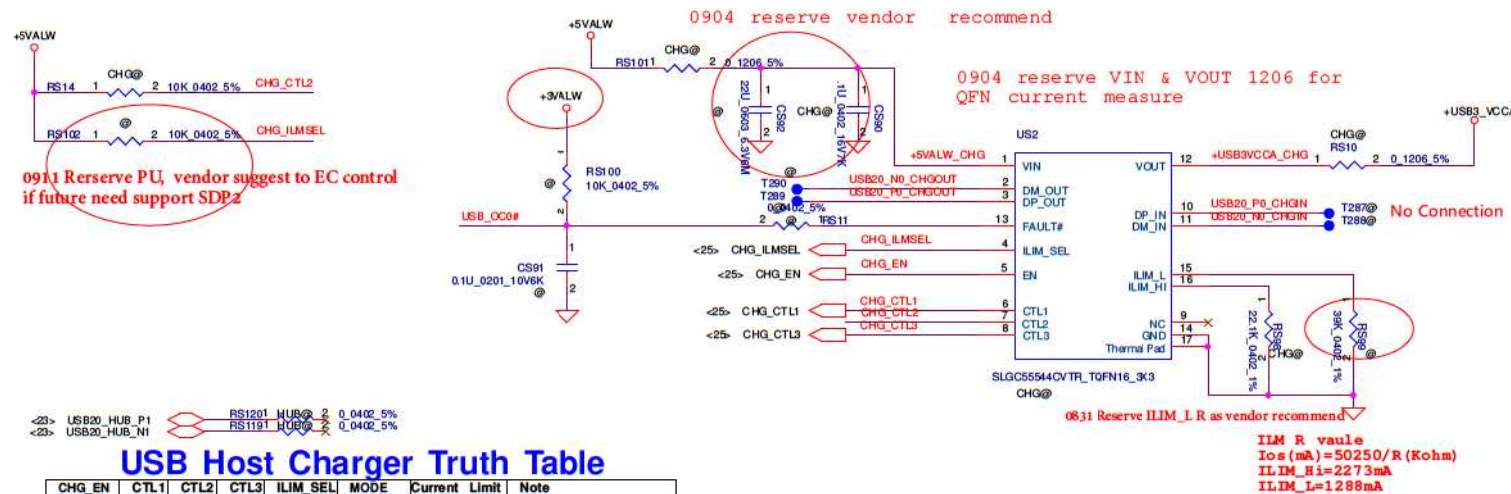


## USB3.0 (Port 0)

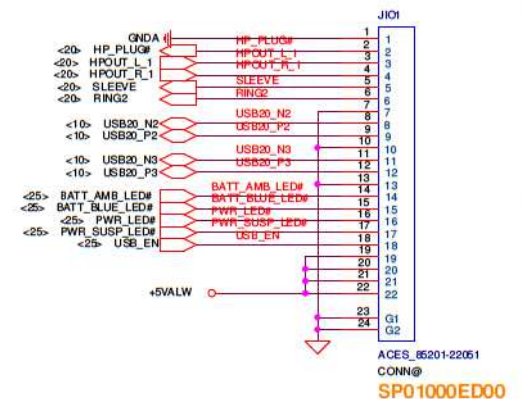


## USB Host Charger (Reserved)

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## USB/B (USBx2, AUDIO, LEDx2)

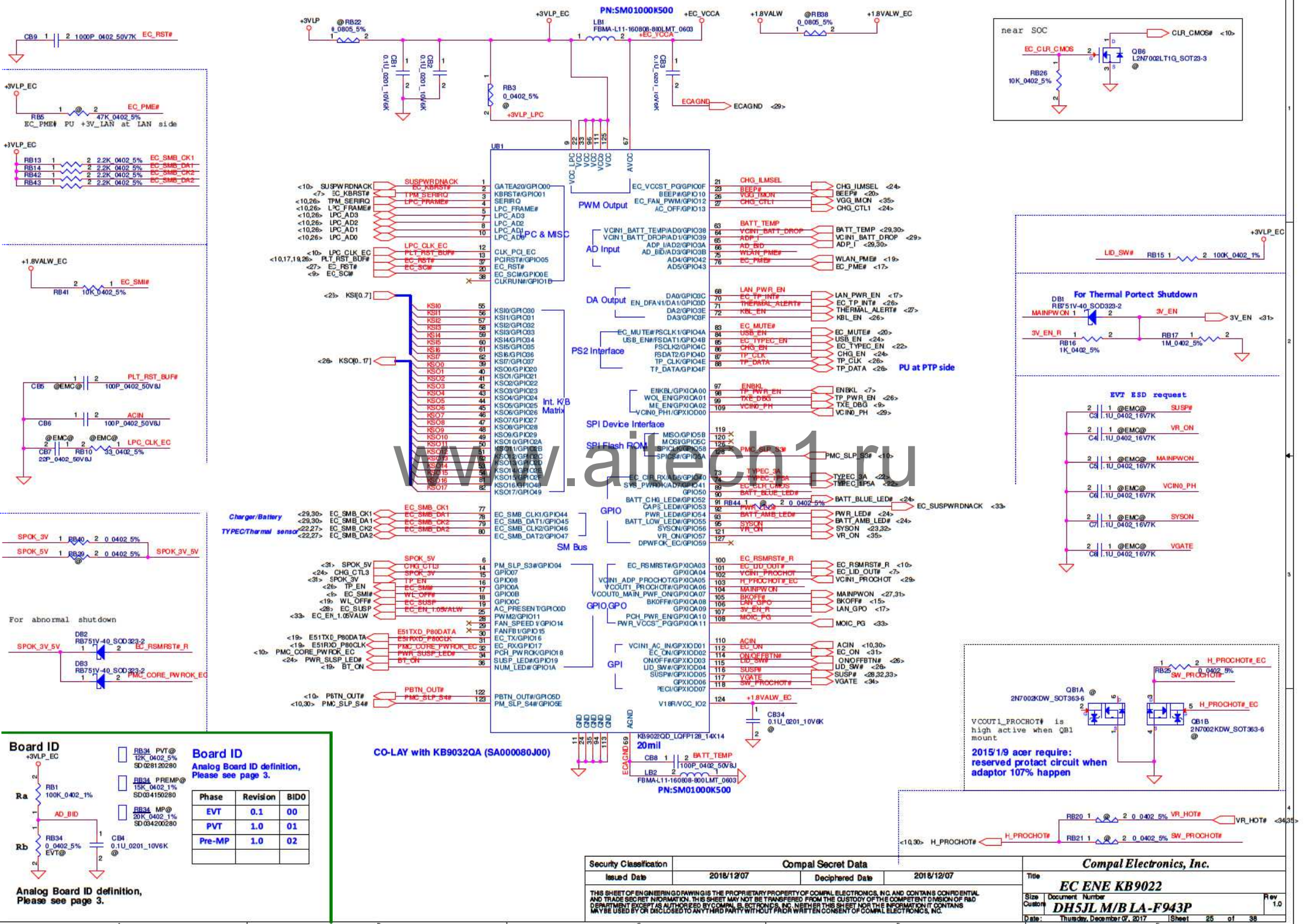


## USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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**Board ID**  
+3VLP\_EC

RB34 PVT@ 12K\_0402\_5% SD 028120280

RB34 PREMP@ 15K\_0402\_1% SD 034150280

RB34 MP@ 20K\_0402\_1% SD 034200280

**Analog Board ID definition, Please see page 3.**

Phase	Revision	BID0
EVT	0.1	00
PVT	1.0	01
Pre-MP	1.0	02

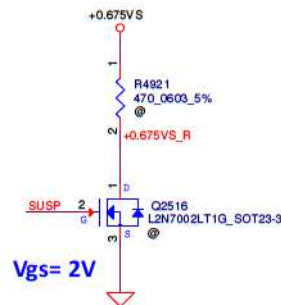
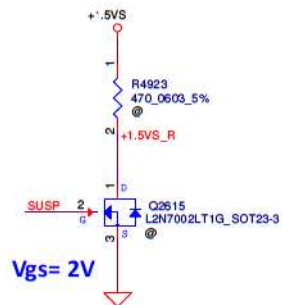
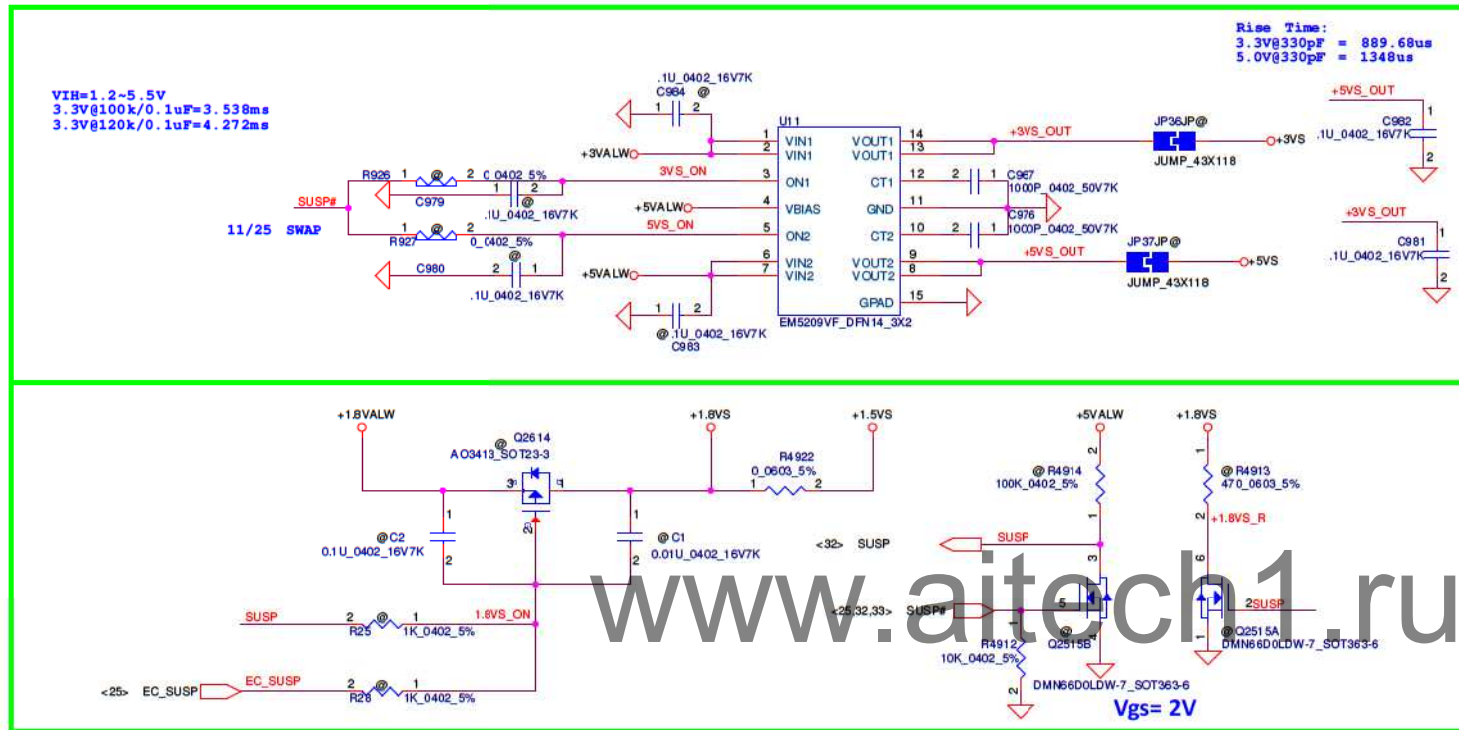
CO-LAY with KB90320A (SA000080J00)



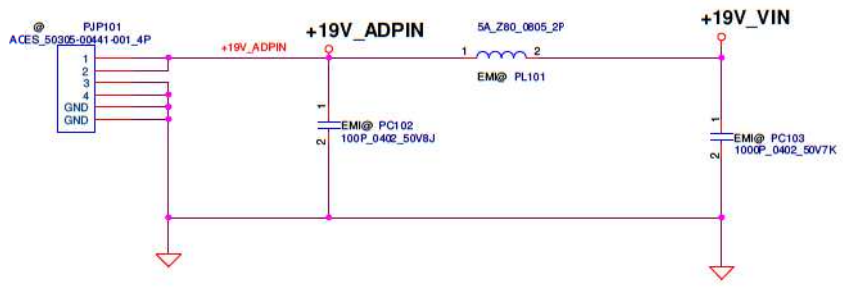




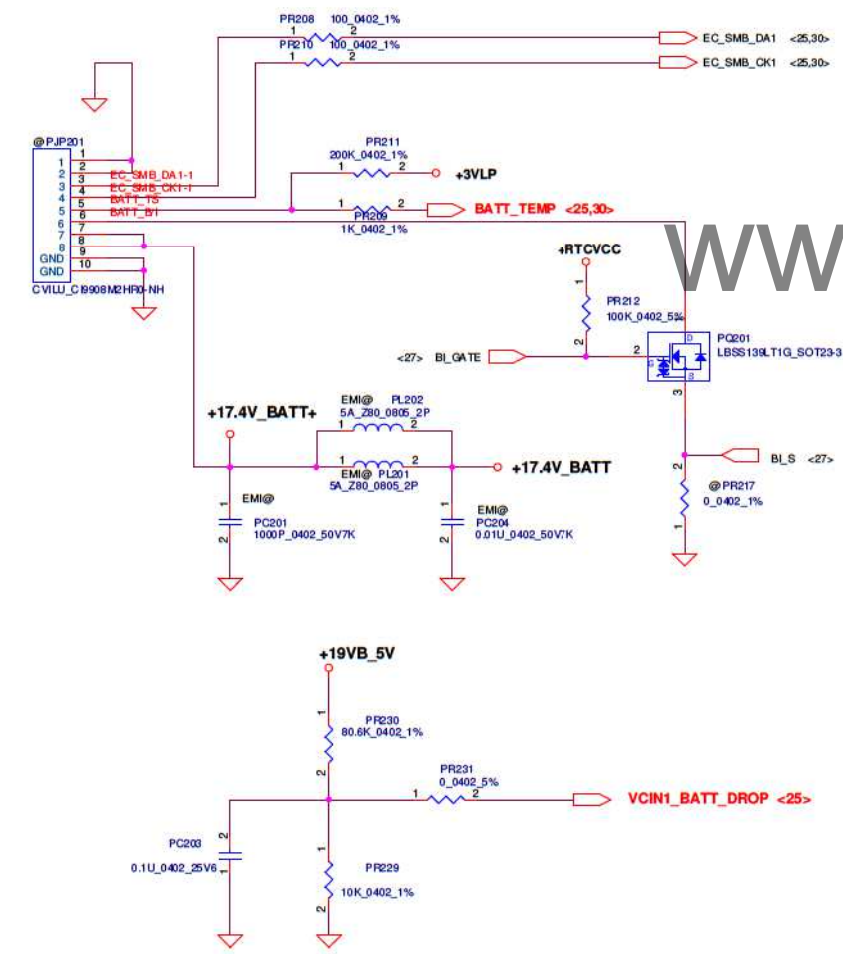
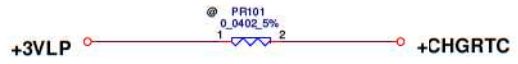
## DC Interface



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				DC INTERFACE	
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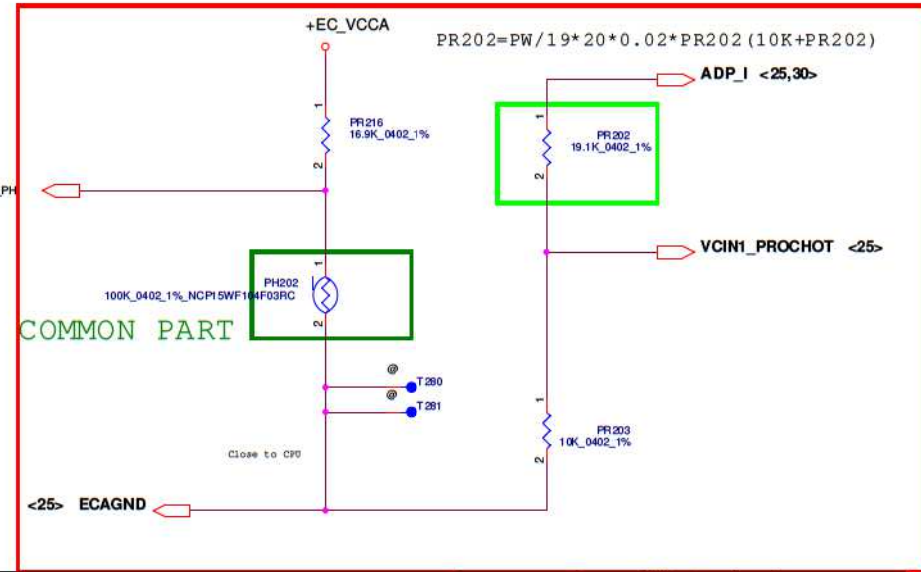
PVT:Delete PH2 thermal sensor



	For KB9022 OTP
9 2 °C	1.0V
5 6 °C	2.0V
PR216	16.9K ohm

Need confirm the setting

For KB9022 sense 10mΩ	Active	Recovery	PR202
45W	0.339V (58.5W)	0.339V (58.5W)	19.1KΩ



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max Power loss 0.22W for 90W; 0.12W for 65W system; 0.05W for 45W  
CSR rating: 1W  
VCSP-VCSPIN spec < 81mV

Protection for reverse input

Vgs = 20V  
Vds = 60V  
Id = 250mA

Need check the SOA for inrush

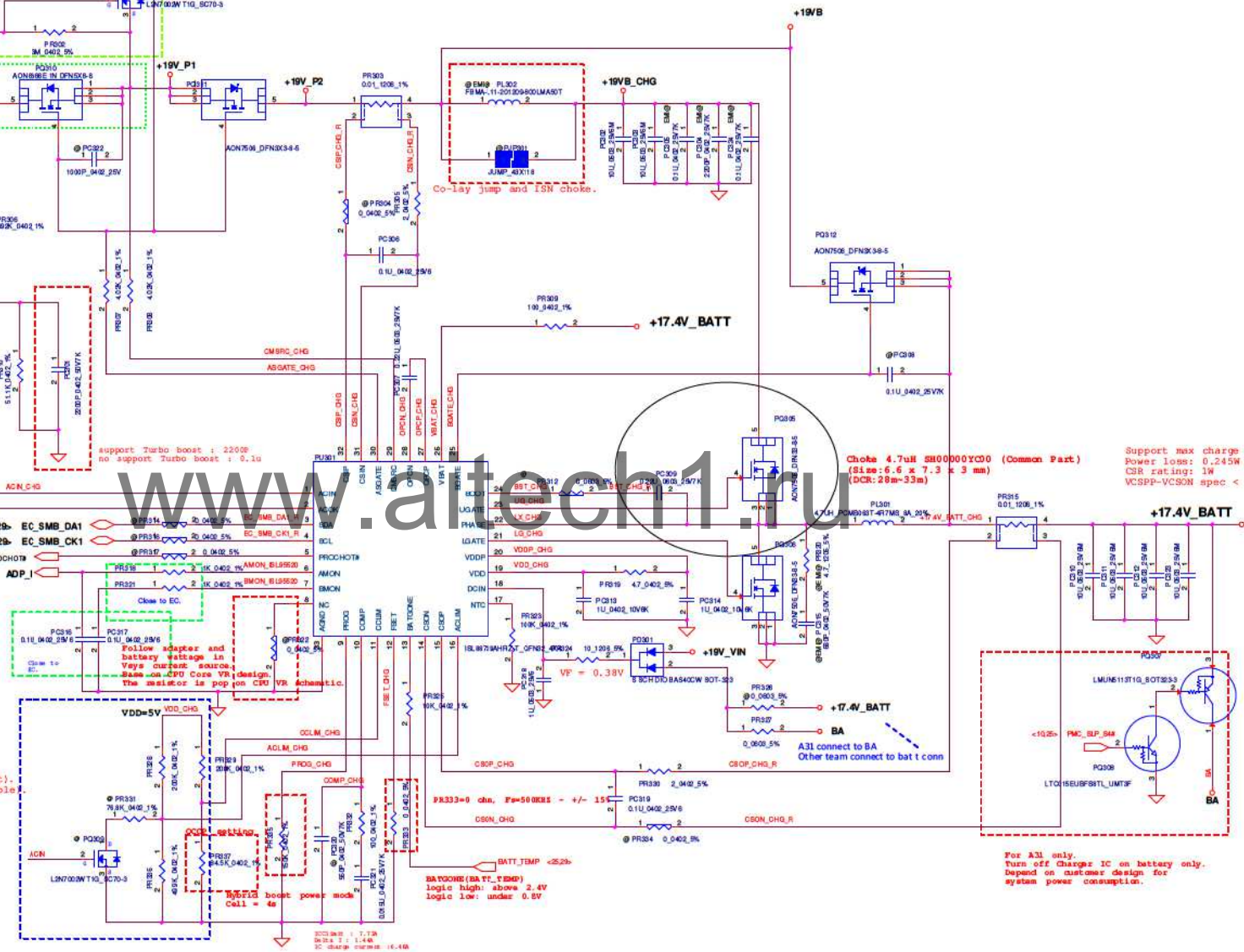
Range: 2V-3.5V  
20\*19.9/(392+9.9)=2.55V

0x3CH <BIT> PRS current gain  
Rd1 = 10mΩ and Rd2 = 5mΩ or Rd1 = 10mΩ and Rd2 = 1mΩ  
BIT0 = 1.14uA/W  
BIT1 = 0.285uA/W  
By BIT1,  $\eta_{\text{eff}} = 2.5\text{mW/W}$  (VADP \* IADP + VBAT \* IIR)  
R\_Pays = 1.2V / I\_Pays  
VSDYS = 1.14uA/W  
adaptor wattage = 45W  
Battery wattage = 40W  
I\_Pays = 1.14 A (45+40) = 96.9uA  
R\_Pays = 1.2V / 96.9uA = 12.38-ohm  
=====  
Rd1 = 20mΩ and Rd2 = 10mΩ or Rd1 = 20mΩ and Rd2 = 2mΩ  
BIT0 = 2.28uA/W  
BIT1 = 0.57uA/W  
adaptor wattage = 45W  
Battery wattage = 40W  
I\_Pays = 1.14 A (65+40) = 119.7uA  
R\_Pays = 1.2V / 119.7uA = 10.08-ohm

**\*\*Design Notes\*\***  
For 45W/65W/90W system, 2S/3S/4S battery  
Maximum Charging current 3.5A  
Maximum Battery discharge power 55W  
Register Setting  
1. 0x3DH bit10 set 0 (default 1) to enable turbo boost function  
2. Disable turbo when AC only  
Circuit Design  
1. ACLIM and CCLIM are divider voltage control.  
2. Use TX7 choke and X3 H/L side MOSFET  
Charge current 3A  
Power loss = 1.79W (H/S=0.227W, L/S=1.273W, Choke=0.297W)  
Power density = 0.61 (23X16)  
Protect function  
1. ADOVP: VDD voltage > 24V  
2. SMBus timeout: 0x3DH bit15 set 0 (default 0) to enable 175s (default).  
3. ACOC: 0x3CH bit4 set1 release adapter limit function (default:Enable)  
4. CHOCOP: based on charge current setting  
5. BATOVF: 4.6V/Cell  
6. BATLOW: No.  
7. TSHUT: 150C

Battery current limited by CCLIM = 3.89A.  
Adaptor current limited by ACLIM = 4.33A.  
(PR779 and DQ741 are for change ACLIM when AC in)

(Rd1 = 10mΩ and Rd2 = 5mΩ or Rd1 = 20mΩ and Rd2 = 10mΩ)  
CC\_31m = Vcc31m / 64 \* Rd2  
(Rd1 = 10mΩ and Rd2 = 10mΩ or Rd1 = 20mΩ and Rd2 = 20mΩ)  
CC\_32m = Vcc32m / 32 \* Rd2  
=====  
AC\_33m = Vcc33m / 32 \* Rd1



Support max charge 3.5A  
Power loss: 0.245W  
CSR ratings: 1W  
VCSP-VCSPIN spec < 81mV

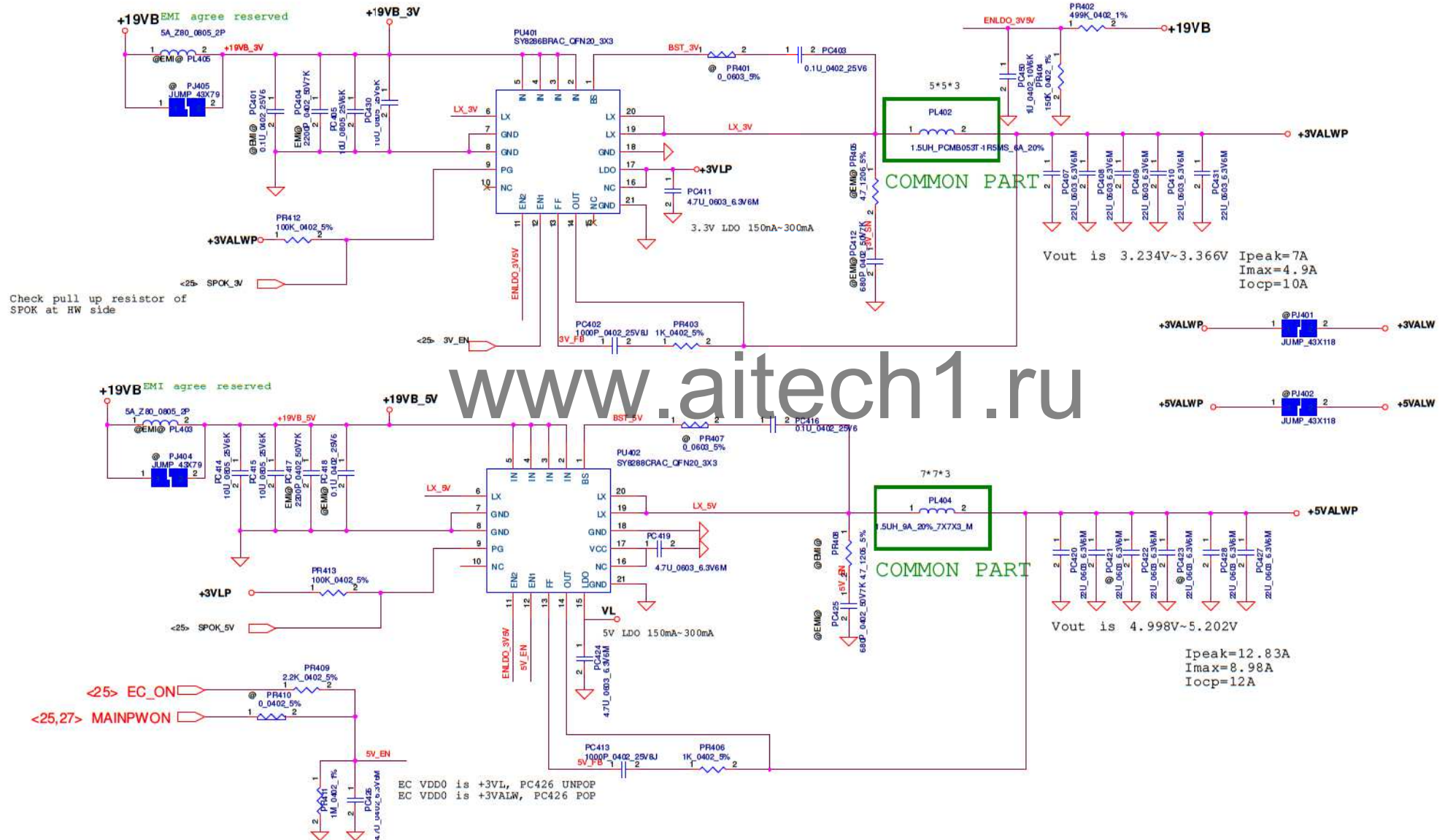
For A31 only.  
Turn off Charger IC on battery only.  
Depend on customer design for  
system power consumption.

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# Module model information

SY8208B\_V2.mdd

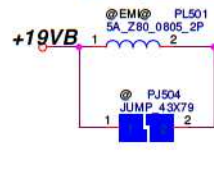
SY8208C\_V2.mdd



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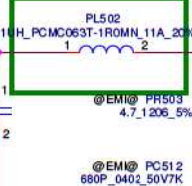
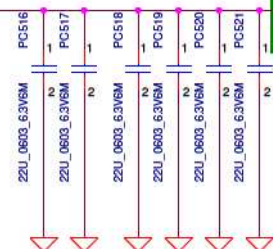


EMI agree reserved



7\*7\*3  
COMMON PART

+1.35VP

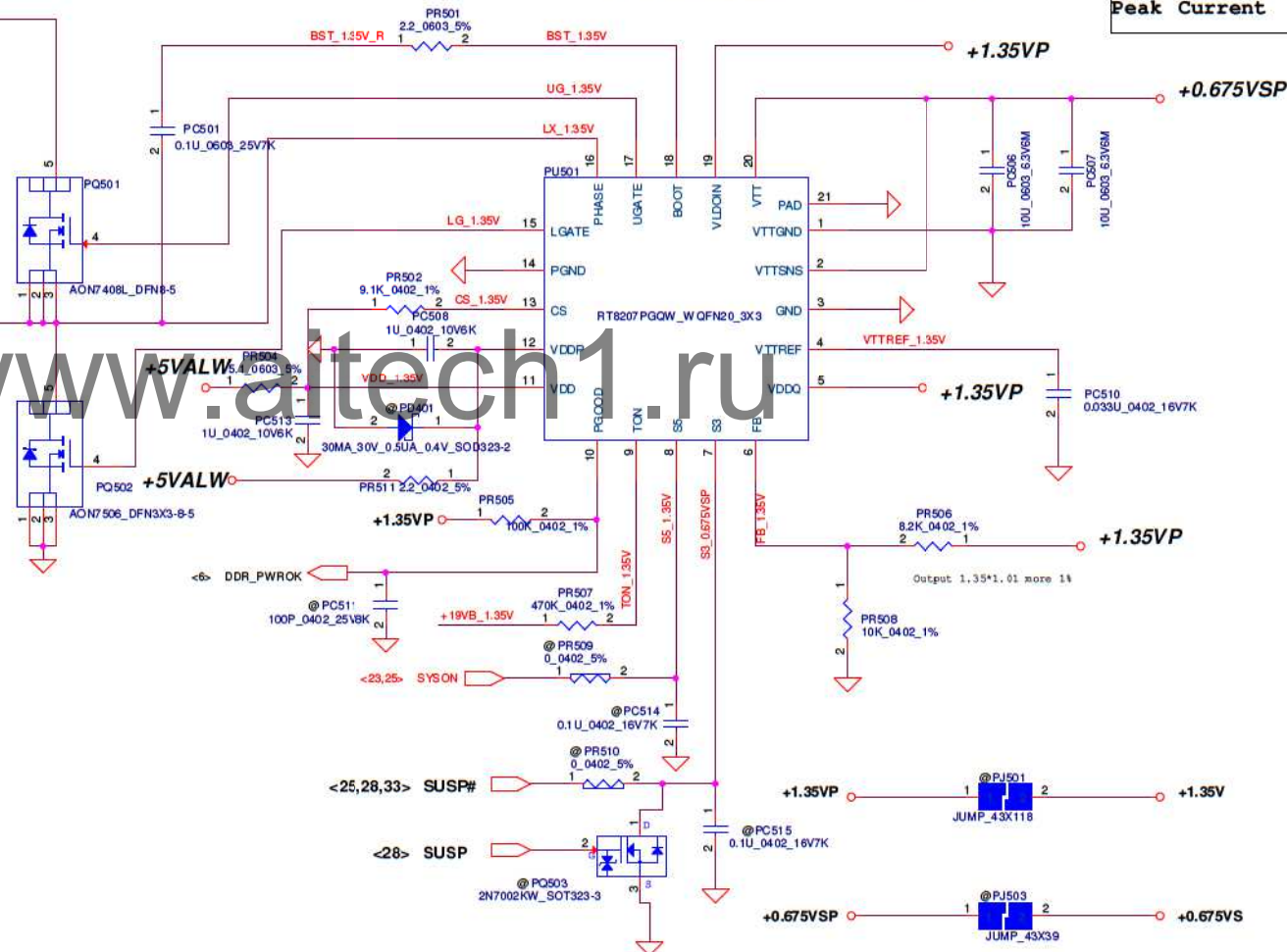


Mode Level +0.675VSP VTTREF\_1.35V  
S5 L off off  
S3 L off on  
S0 H on on  
Note: S3 - sleep ; S5 - power off

Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.84A  
Peak Current 1.2A

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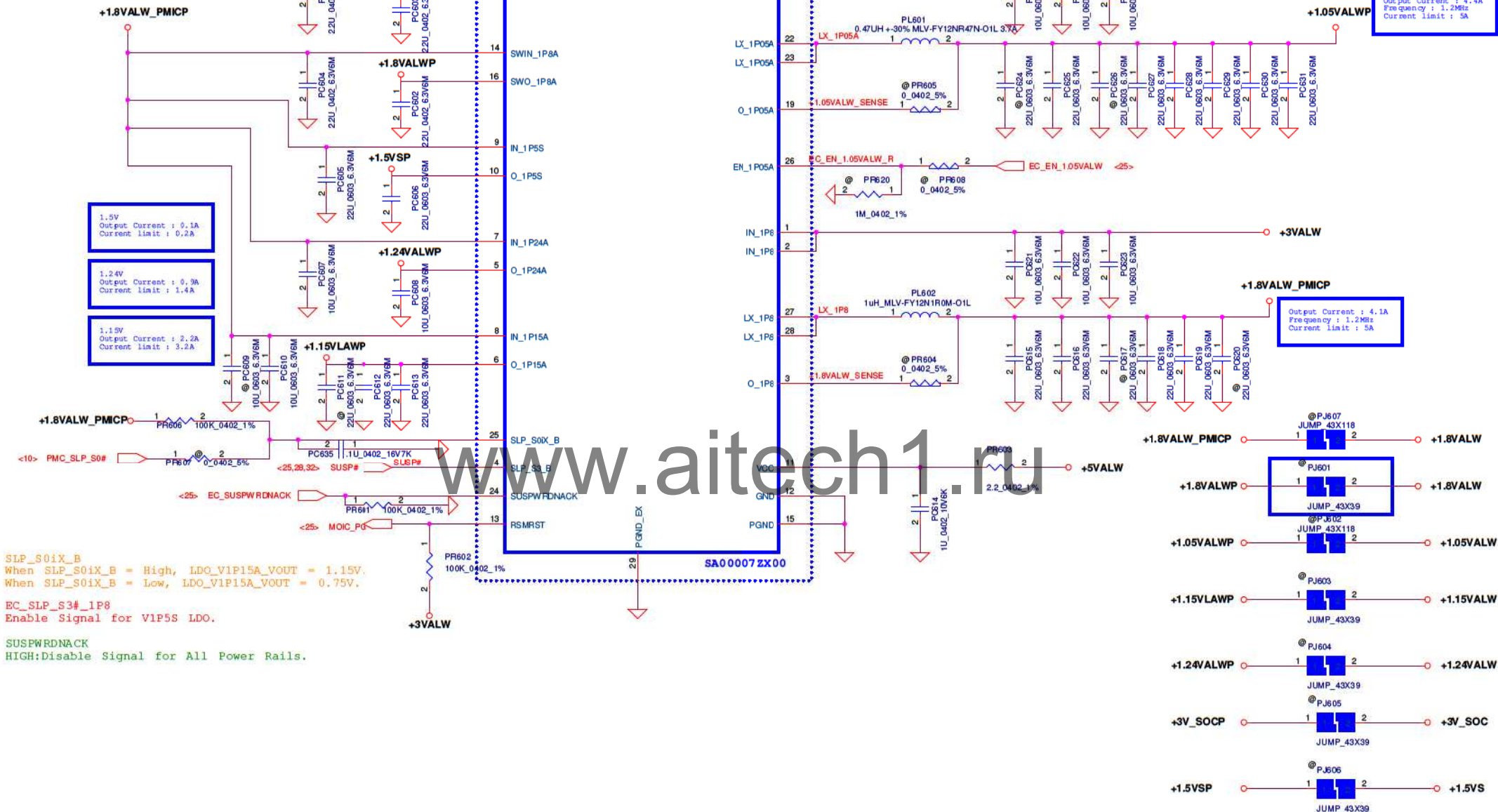
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## Function Field :

Regulator 35.5

Support 35.6



SLP\_S0iX\_B  
When SLP\_S0iX\_B = High, LDO\_V1P15A\_VOUT = 1.15V.  
When SLP\_S0iX\_B = Low, LDO\_V1P15A\_VOUT = 0.75V.

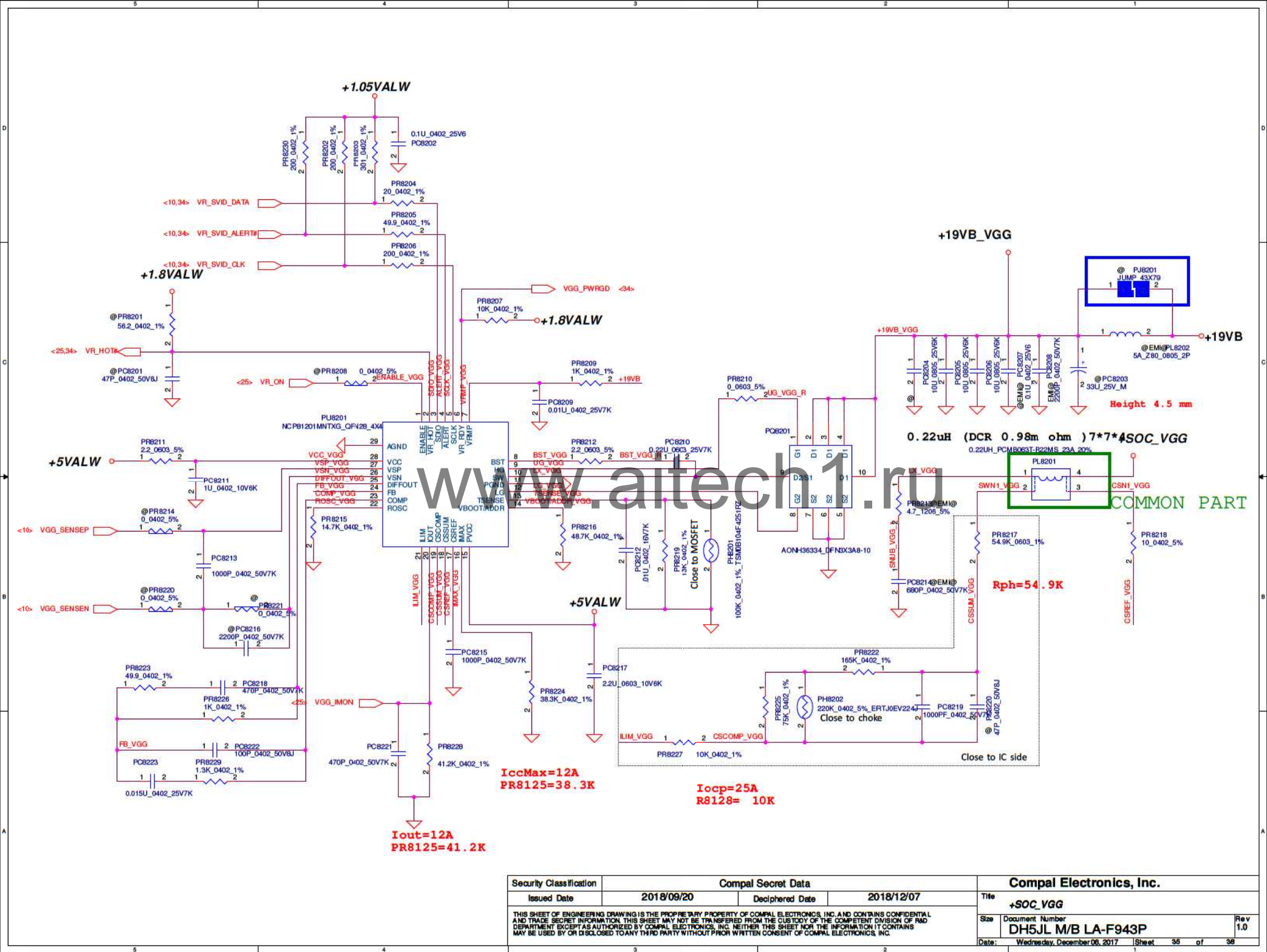
EC\_SLP\_S34\_1P8  
Enable Signal for V1P5S LDO.

SUSPWRDNACK  
HIGH:Disable Signal for All Power Rails.

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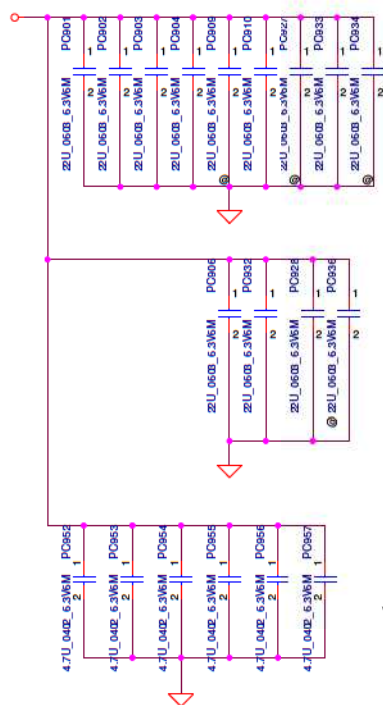






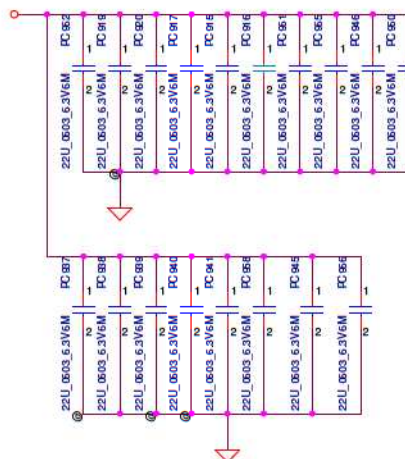
4.7U\_0402 \* 6 +22U\_0603 \* 9+ 4 reserved

+SOC\_VCC



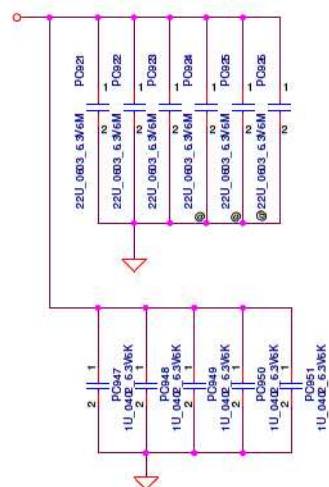
22U\_0603 \* 14 + 4 reserved

+SOC\_VGG



1U\_0402 \* 5 + 22U\_0603\*3 + 3 reserved

+1.05VALW



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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev
1	19	WLAN	11/13	Pin18 connect to power ,can't work normally	Pin18 connect to GND	EVT	0.1
2	20	Audio	11/14	DVDD/IO connect to 3V ,cant work normally	DVDD/IO change to 1.8VS for SOC HDA level	EVT	0.1
3	10	SOC	11/17	KB can't work normally	U71 Pin6 connect to 3VLP_EC	EVT	0.1
4	16	HDMI	11/22	HDMI DCC can't work normally	Delete one LS / HPD signal cancel PU resistor	EVT	0.1
5	26	TPM	11/23	TPM power leakage	TPM power from VS change to VALW	EVT	0.1
6	19	WLAN	11/29		Add RM7 connect to 3VALW for reserved	EVT	0.1
7	20	Audio	11/29	DA5 over z-limit	For move BOT side, exchange Pin2/Pin3	EVT	0.1
8	21	SSD	12/4		Add SATA SSD conn and SSD DET# for reserved	EVT	0.1
9	21	SSD	12/4		SATA SSD /HDD exchange port/add R1007	EVT	0.1

1.0

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